SHARP
SERVICE MANUAL

PC-1500

WWW.
PC-1500
.INFO

MODEL-PC-1500

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

(1) Key layout

Adaptor jack
Used to supply power from AC line via the EA-150
AC Adaptor that comes with the option unit, CE-150.

SOFT KEY   DISPLAY   SHIFT KEY

150:C=√(A*A+B*B−2*A*B*COS

SHARP

KEYBOARD   ENTER KEY   MODE KEY
                  (Key to start program   CLEAR/CLEAR ALL KEY
                  execution or entry)   POWER ON/BREAK KEY
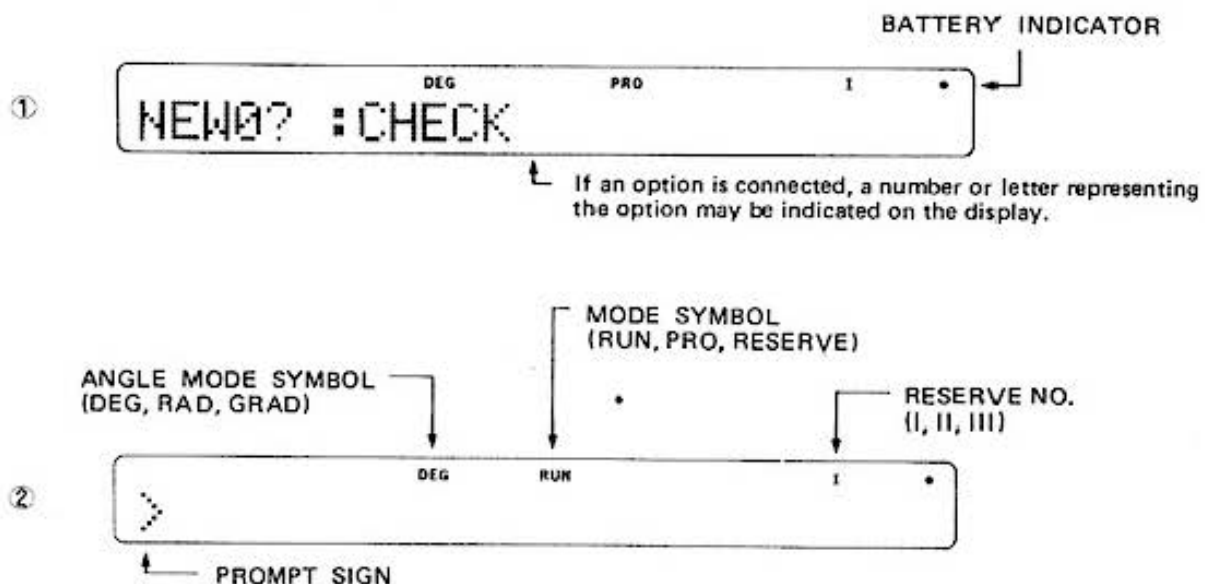   POWER OFF KEY
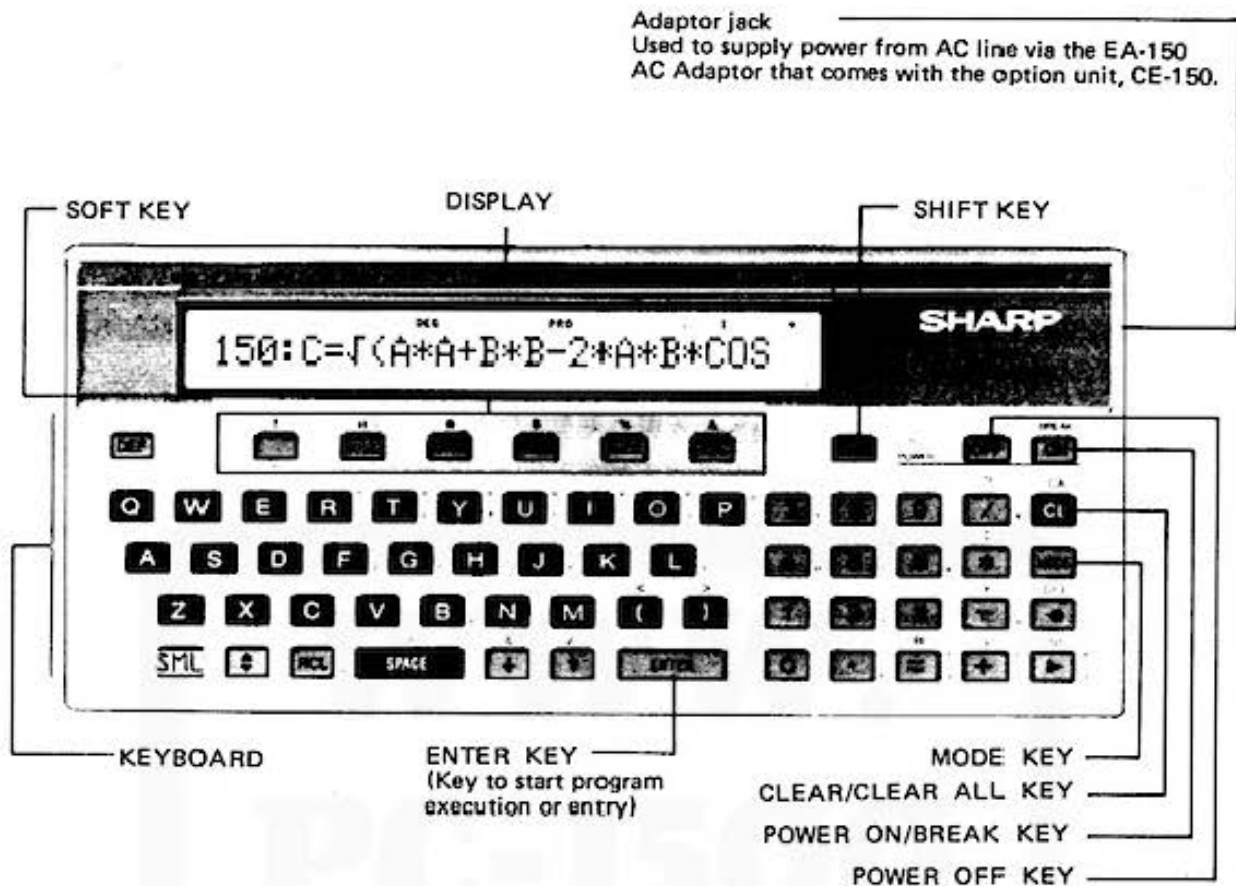
● Kinds of keys
   There are 65 keys in all, and their functions differ depending on how whether operation is per-
   formed operated, independently or in conjunction with the SHIFT key.

(2) Power on/off

Depression of the ON key that is located on the upper right corner of the keyboard causes the
power to turn on and the following prompt appears on the display.

BATTERY INDICATOR

①
NEW0? :CHECK

DEG   PRO   I   •

If an option is connected, a number or letter representing
the option may be indicated on the display.

MODE SYMBOL
(RUN, PRO, RESERVE)

ANGLE MODE SYMBOL
(DEG, RAD, GRAD)   RESERVE NO.
                                                       (I, II, III)

②
>
DEG   RUN   I   •

PROMPT SIGN

1

The prompt shown in (1) appears after an operation such as battery replacement.

The pocket computer needs to be reset in the following manner, when the prompt shown in (1) appears on the display.

CL NEW 0 ENTER "NEW 0" is the command to reset all pocket computer conditions to their initial states.

Upon completion of above operation, the prompt sign shown in (2) is brought on the display.

Also, depressing the ON key after turning off the power with the OFF key brings the same prompt on the display.

However, involvement of a failure in a peripheral will put a check message such as "CHECK 6" on the display, if any peripheral is connected to the pocket computer.

- ● Auto power off

  With this pocket computer the power is automatically shut off to save power, unless a key entry is made within seven minutes after the last key entry.

  Depression of the ON key after automatic turn-off turns the power on to the pocket computer, then the machine and display conditions return to what they were imediately before the power was shut off.

(3) Specifications

Capacity:	10 digits (mantessa) + 2 digits (exponent)
Operating sequence:	Direct formula entry (furnished with priority determining function)
Programming language:	BASIC
Central processing unit:	CMOS 8-bit microprocessor
Memory configuraton:	ROM: 16KB
	RAM: 3.5KB

	System area:	0.9KB
	Input buffer area:	80 bytes
	Stack area:	196 bytes

Power consumption:	0.13W
Physical dimensions:	195(W) x 86(D) x 25.5(H)mm
Weight:	375g, including batteries
Accessories:	Soft case, two templates, four batteries (type AA), instruction manual, applications manual and name label.

(4) Options

- ● **CE-150 color graphic printer (built-in cassette interface)**

  The CE-150 is the 4-color graphic printer that incorporates the cassette interface unit. As ball point pen type of stylus is used for printing, four varieties of colored pens (black, blue, green, red) can be installed and controlled by the program to draw either a straight or broken line from any desired location by the color designated. Combinations of colors and lines will enable the formation of colorful graphics and any desired figure. The CE-150 can also be used to print program lists and data outputs.

  Two tape recorders may be connected at the same time with the CE-150, one can be used for recording and the other for data transfer. For instance, today's data can be summarized and recorded in one tape recorder, while transferring the data file of yesterday from the other tape recorder.

- ● **CE-151 memory module**

  The CE-151 is the RAM chip of 4KB used to expand the program and data storage of the PC-1500.
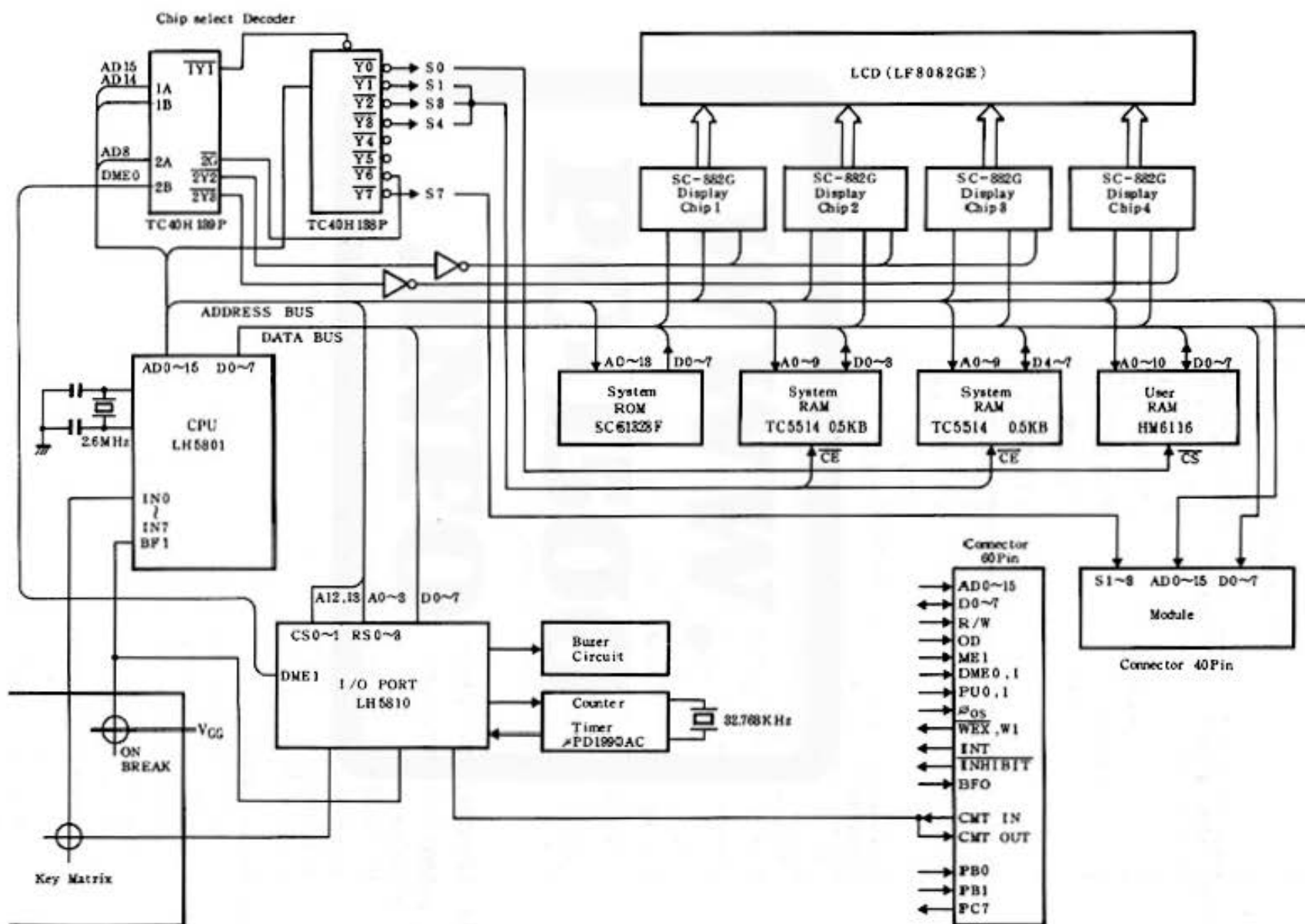
  - ○ When the CE-151 is mounted in the PC-1500, the capacity of program and data storage is expanded to 5946 bytes.
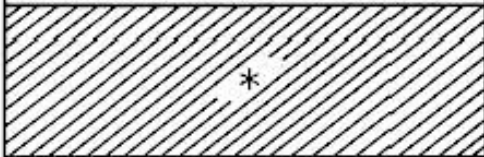
- ● **CE-152 cassette tape recorder**

  The CE-152 is the cassette tape recorder exclusively designed for use with the pocket computer. Storing previous program and data on tape using the CE-152 as the external memory device of the PC-1500 will enable you to use the data again.

2   Note that it needs the CE-150 color graphic printer to use the CE-152 cassette tape recorder.

2. BLOCK DIAGRAM

Chip select Decoder

AD15
AD14
1A
1B
1Y1

AD8
DME0
2A
2B
2Y2
2Y3
2Y2
2Y3

TC40H189P

Y0 — S0
Y1 — S1
Y2 — S8
Y8 — S4
Y4
Y5
Y6
Y7 — S7

TC40H188P

LCD (LF8082GE)

SC–882G Display Chip 1
SC–882G Display Chip 2
SC–882G Display Chip 8
SC–882G Display Chip4

ADDRESS BUS
DATA BUS

AD0~15 D0~7

CPU
LH5801

2.6MHz

IN0
~
IN7
BF1

A0~18 D0~7
System ROM SC61328F

A0~9 D0~8
System RAM TC5514 0.5KB

A0~9 D4~7
System RAM TC5514 0.5KB

A0~10 D0~7
User RAM HM6116

CE   CE   CS

S1~8 AD0~15 D0~7
Module

Connector 40Pin

A12,I3 A0~3 D0~7

CS0~1 RS0~8

DME1   I/O PORT
LH5810

Buzer Circuit

Counter Timer μPD1990AC

32.768KHz

VGG

ON
BREAK

Key Matrix

Connector 60Pin

AD0~15
D0~7
R/W
OD
ME1
DME0,I
PU0,1
⌀os
WEX,W1
INT
INHIBIT
BFO

CMT IN
CMT OUT

PB0
PB1
PC7

3

2-1. RAM MAP

```
                                    0000
            USER MEMORY                          Y0
                                    3FFF
2KB  USER MEMORY STANDARD           4000  ] S0
                                    47FF
                                    4800  ) S1
            USER MEMORY             5000  ) S2
            OPTION                                Y1
            10KB                    5800  | S3
                                    6000  ) S4
                                    6800  ) S5
                                    7000  )
                    *               7200    S6
                                    7400  )
      Display chip 1 , 3            7600
      Display chip 2 , 4            7700
      System Memory                 7800  )
                    *               7C00    S7
      PV          PV                8000
      EXPAND      EXPAND                         Y2
      ROMⅡ 16KB   ROMⅠ 16KB          BFFF
      SYSTEM                        C000
                                                 Y3
      POGRAM 16KB                   FFFF
```

$*$: Inhibit to use by redundancy

2-2. LSI signal description

1. LH5801 (8-bit CMOS MPU)

1) Outline

The LH5801 is the 8-bit microprocessor of the CMOS static type, featuring very low power dissipation and large data processing capability. The MPU incorporates functions such as the LCD backplate signal generator, input port, external latch clock, and timer, which allows a variety of systems with a few chips.

2) Features of MPU

- ○ 8-bit parallel operations
- ○ 128KB direct accessing
- ○ Implementation of 6-byte general purpose register besides the accumulator allows the use of three data pointers.
- ○ 9-bit timer function
- ○ Three kinds of interrupts
    Non-maskable interrupt
    Maskable interrupt
    Timer interrupt
- ○ Instruction set of 80 kinds
- ○ DMA and multiprocessor capabilities
- ○ MPU wait function (memory access control)
- ○ Implementation of 8-bit input port and clock Pϕ for external latch

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○ Memory backup function
○ LCD back plate controll
○ Clock 2.6MHz (crystal control)
  Internal machine cycle 1.3MHz
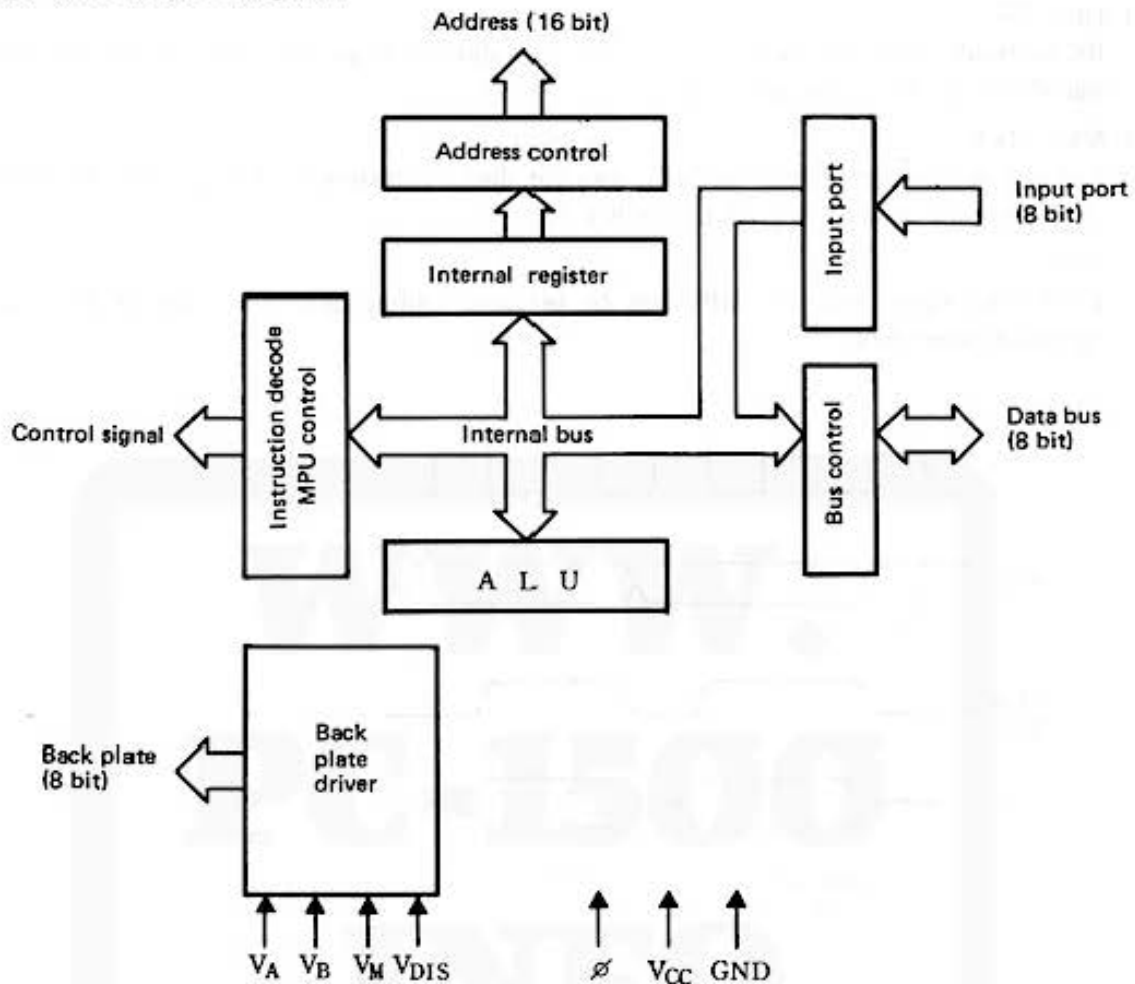 Mininum instruction excute time ...... $1.3\mu S$

2-3. MPU block diagram

Table below shows the internal registers of the MPU that consist of 8-bit x 14 RAM storages.

P_H	P_L	...... Program counter	
S_H	S_L	...... Stack pointer	Exclusive registers
W_H	W_L	...... W register	
A	E	...... A register, E register	
U_H	U_L	...... U register	
Y_H	Y_L	...... Y register	General purpose register
X_H	X_L	...... X register	

MPU registers consists of two groups of registers; exclusive register group and general purpose register group.

Exclusive registers consist of program counter (PH, PL) [16 bits], stack pointer (SH, SL) [16 bits], and W register (WH, WL) [16 bits].

General purpose registers consist of eight 8-bit registers; U register (UH, UL), X register (XH, XL), and Y register (YH, YL) can be used in pair to comprise 16-bit registers.

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2-4. Pin description

(1) **XL0, XL1**

Crystal oscillator external connection pins (XL0: In, XL1: Out)

(2) **AD0 ~ AD15**

16 bits address bus (AD0: least significant address bit, AD15: most significant address bit). Turns high impedance by the BRQ signal.

(3) **D0 ~ D7**

Bidirectional data bus used to write and read data to/from the external memory (D0: least significant bit, D7: most significant bit).

(4) **ME0, ME1**

Memory enable signals that the MPU uses for direct accessing to an external memory of which the maximum capacity is 128KB (64KB x 2).

(5) **R/W**

Read/write signal that the MPU use to perform reading operation when R/W=1 and write operation when R/W=0.
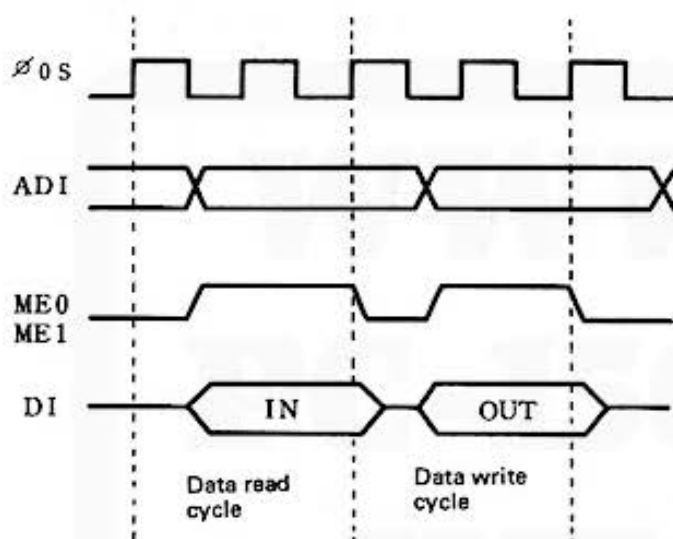
(6) **RESET**

A high input of this signal causes the MPU to return to its initial state.

(7) **BRQ**

Bus request. A high state of this signal causes the MPU to respond with the high state of the BAK signal upon completion of present command execution.

(8) **BAK**

Bus acknowledge appears in response with a high BRQ indicating that address bus, data bus, R/W, ME0, and ME1 are in high impedance.

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(9) OPF

Operation code fetch appears when the MPU fetches an operation (instruction) code. OPF is an output only during the fetch of an instruction code and is not an output when address data, immediate data, or the second byte of a two step instruction is fetched.
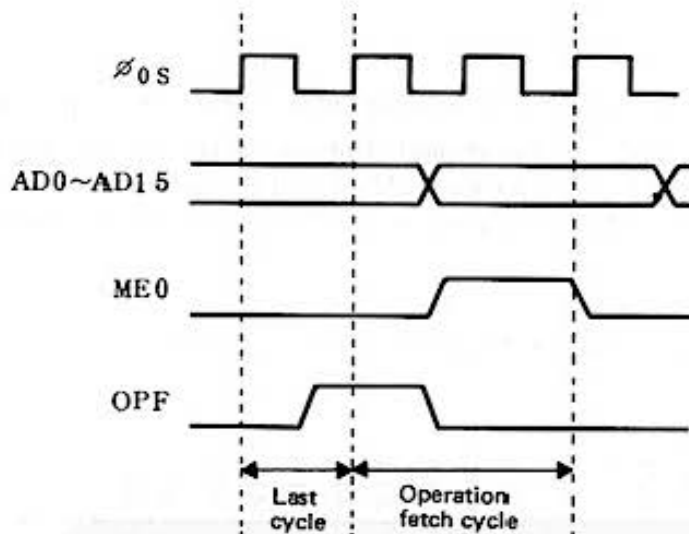
(10) IN0 ~ IN7

Input port. The MPU takes the signal on IN0 ~ IN7 input port into the internal accumulator as 8-bit data.

(11) PU, PV, DIS

On chip flipflops of which outputs are on LSI pins.
PU: Set to high with the SPU instruction and set to low with the RPU instruction.
PV: Set to high with the SPV instruction and set to low with the RPV instruction.
DIS: Set to high with the SDP instruction and set to low with the RDP instruction.

(12) Pϕ

Strobe output is an output during the execution of the ATP instruction normally, used for the external latch of the A register contents.

(13) ϕOS

Clock which is in the same phase as the basic clock inside the chip and it is the basic clock for an entire system.
It becomes the basic clock of 1.3MHz frequency when a 2.6MHz crystal is connected between XL0 and XL1.

(14) WAIT

WAIT output that informs the MPU that addressed memory or I/O device is not ready. The MPU is in the wait state while this signal is on.

(15) H0 ~ H7

LCD backplate signal

(16) VA, VB, VM, VDIS

LCD drive source.

(17) HIN

LCD backplate signal. Counter input that generates H0 ~ H7. Normally connected to HA.

(18) HA

MPU divider output.

(19) BFO, BFI

MPU internal register BF flipflop output (BFO) and input (BFI) can be reset by the instruction from the MPU and set by the BFI input. Normally used for the memory backup system.
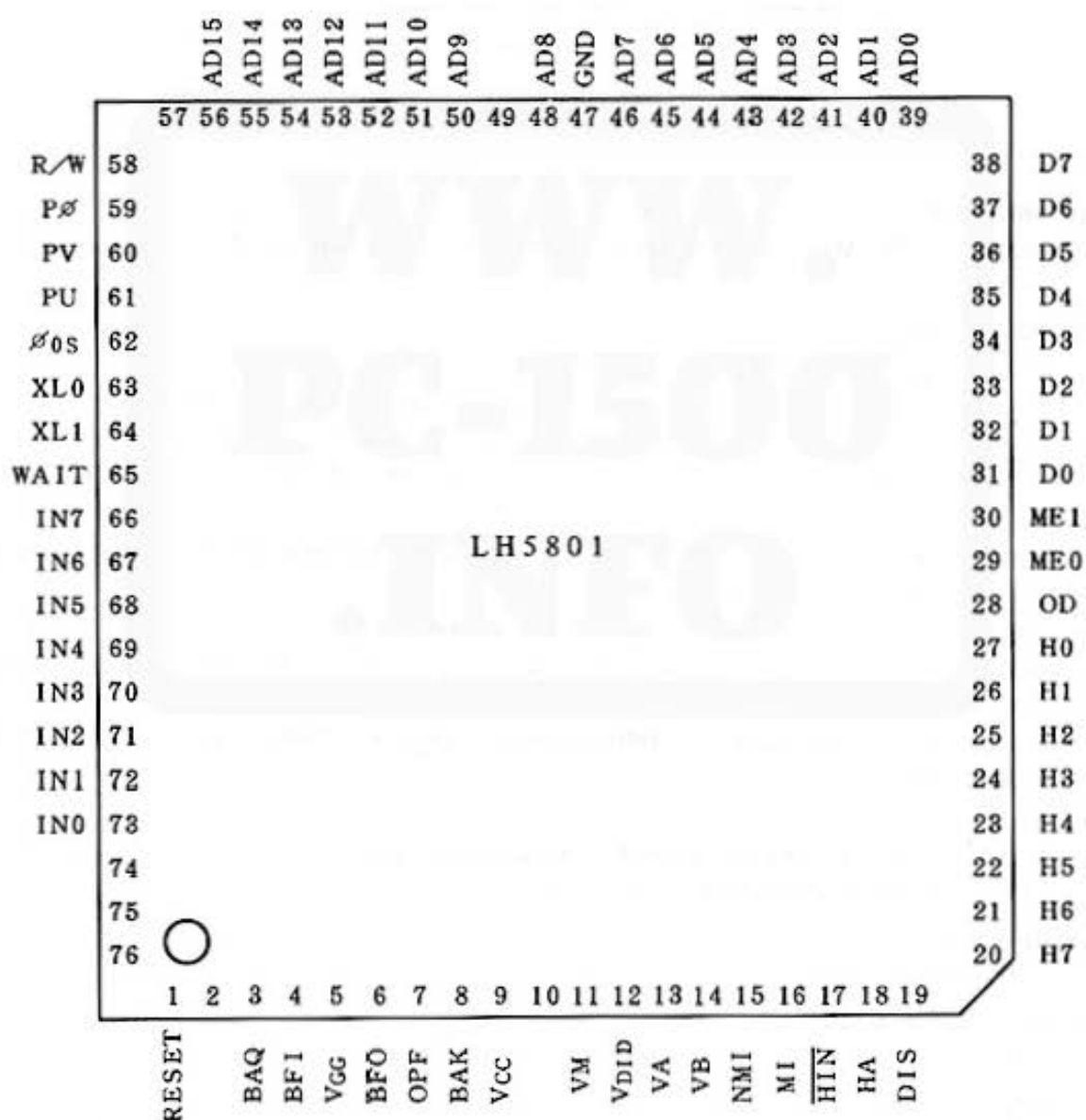
7

(20) NMI

Non-maskable interrupt. A high NMI signal denotes an interrupt request, to which the MPU responds unconditionally and the control moves to start the interrupt processing routine after the contents of the memory address FFFC is moved into the high order byte of the program counter and the contents of the memory address FFFD into the low order byte of the program counter.

(21) MI

Maskable interrupt. A high on this signal makes interrupt request when interrupt enable is set. The MPU responds unconditionally to this request. Control moves to start the interrupt processing routine after the contents of the memory address FFF8 is moved into the high order byte of the program counter, the contents of the memory address FFF9 are moved into the low order byte of the program counter.

(22) OD

Output disable. When the OD signal is active the data bus is in the output mode.

Top pins (left to right): AD15 (57), AD14 (56), AD13 (55), AD12 (54), AD11 (53), AD10 (52), AD9 (51), AD8 (50), GND (49), AD7 (48), AD6 (47), AD5 (46), AD4 (45), AD3 (44), AD2 (43), AD1 (42), AD0 (41), ... 40, 39

Left pins: R/W (58), PØ (59), PV (60), PU (61), ØOS (62), XL0 (63), XL1 (64), WAIT (65), IN7 (66), IN6 (67), IN5 (68), IN4 (69), IN3 (70), IN2 (71), IN1 (72), IN0 (73), 74, 75, 76

Center: **LH5801**

Right pins: D7 (38), D6 (37), D5 (36), D4 (35), D3 (34), D2 (33), D1 (32), D0 (31), ME1 (30), ME0 (29), OD (28), H0 (27), H1 (26), H2 (25), H3 (24), H4 (23), H5 (22), H6 (21), H7 (20)

Bottom pins (left to right): RESET (1), BAQ (2), BFI (3), VGG (4), BFO (5), OPF (6), BAK (7), Vcc (8), ... VM (10), VDID (11), VA (12), VB (13), NMI (14), MI (15), HIN (16), HA (17), DIS (18), ... 19

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3. LH5811 I/O PORT

(1) Outline

The LH5811 I/O port is the single chip LSI of CMOS static circuit that can be connected with a general purpose 8-bit CPU. It has the following functions:
 (1) Two pairs of 8-bit bidirectional ports
 (2) One pair of 8-bit output ports
 (3) Two lines of interrupt request inputs, one of them is the input from port.
 (4) One line of interrupt request output.
 (5) CPU wait control
 (6) Serial control

(2) Functions

 (1) Ports, PA0 ~ PA7 and PB0 ~ PB7, can be programmed for I/O directions by each bit.
 The CPU can access PA0 ~ PA7 and PB0 ~ PB7 as though one location of memory.
 (2) PC0 ~ PC7 is the port of output type. The CPU can access it as though one location of memory.
 Also, the latch clock Pφ to the PC port can be supplied directly from an external source.
 (3) LH5811 incorporates two interrupt request inputs, IRQ and PB7, when apply interrupt request to the CPU at the rising edge of the input when the corresponding bit of the internal mask register is "1". Signal PB7 represents the 8th bit of the port PB and it needs to be in the input mode when the interrupt input is applied.

 (4) The LH5811 has a CPU wait control circuit which uses two output lines of memory enable signals for a memory that has slower access time. In addition, two input lines for the wait conditions are used. Six different of access times can be chosen by programming.
 (5) The following functions are provided for serial control.
  A. Serial data transmission
   Serial data transmission is used in the format of start bit/8-bit data/2 stop bits.
   Transmission clock is programmable by changing internal and external clocks, as well as changing the clock rate; 1/1, 1/2, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096 of the basic clock.
  B. Serial data reception
   When a start bit is received in the idle state, 8 bits of data is received, and stored in the internal register and the interrupt request flag is set on.
   Reception clock is sent from the external clock and must be synchronized with the serial data input.
  C. LCD driver control
   The LCD driver is connected with three signal lines of the transmission clock, a serial data bus, and a synchronous signal line to carry out data transfer for chip select, addressing, and data read/write.
   For the transmission clock in this case, the clock rate can be programmed in the same manner as in the serial data transmission clock. (Transmission clock to the LCD driver is 1MHz.)
  D. Pulse waveform
   The pulse waveform can be sentout in continuation. Eight sorts of frequencies are programmable; 1/1, 1/2, 1/128, 1/256, 1/512, 1/1024, and 1/4096 of the basic clock.
  E. Transmission to audio cassette tape recorder
   The modulated signal can be sent from the SD0 output in the format of start bit/8-bit data/2 stop bits.
   Modulation clocks, FX and FY, can be set separately to any of clock rate; 1/64, 1/128, 1/256, 1/512, and 1/1024 of the basic clock.

I/O PORT controller system block diagram
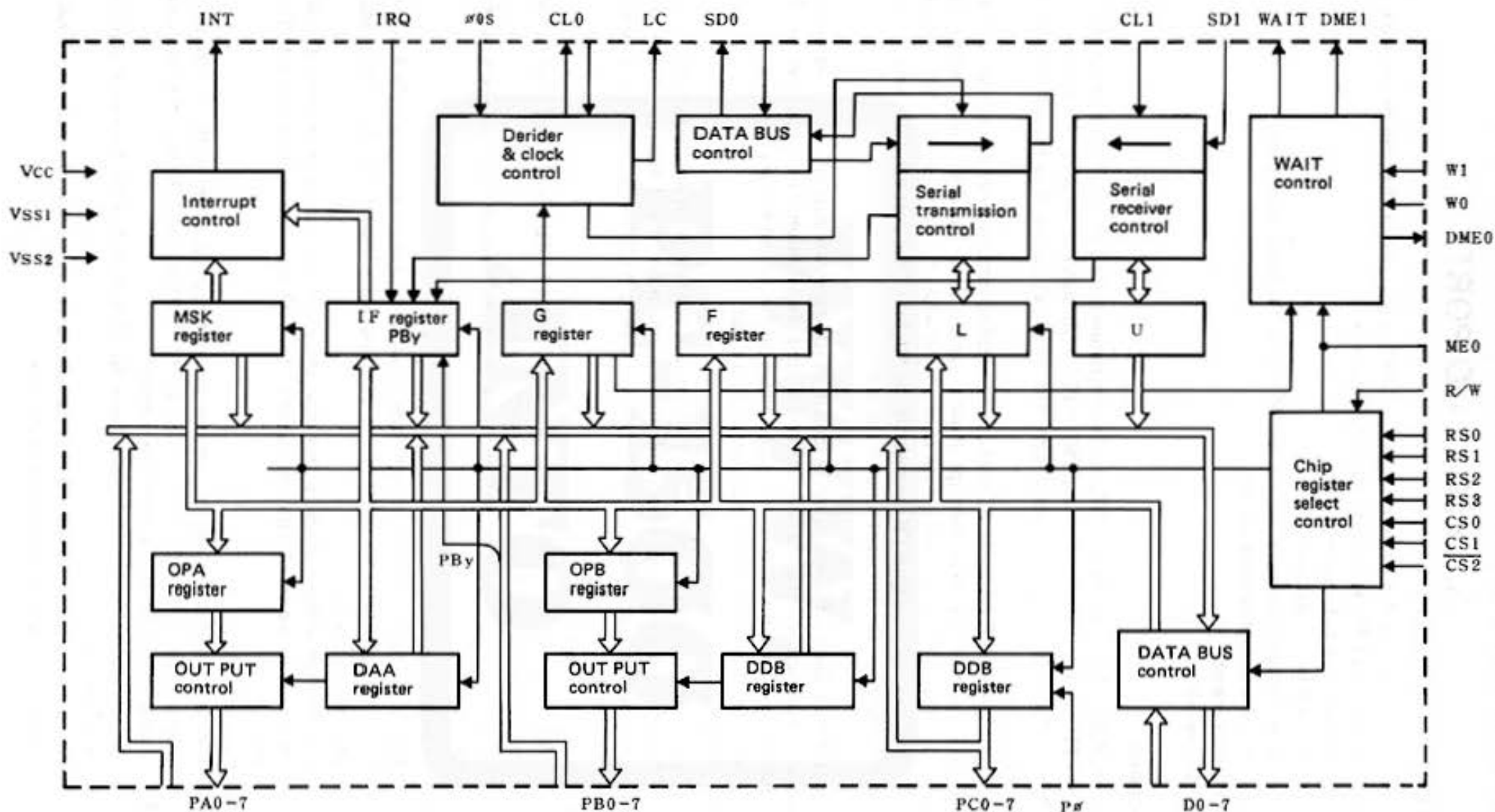
VSS1=VSS2=GND

VCC=4.5±0.5 V

I/O port (LH5810)

Pin No.	Signal Name	In/out	Connection	Functional description
1	PA1	In/out	Key	Port A input/output. Key strobe.
$	$	$	$	$
7	PA7	In/out	Key	Port A input/output. Key strobe.
8	GND	In	Power	0V
9	PB0	In/out	Option	Port B input/output
10	OB1	In/out	Option	Port B input/output
11	PB2	In	CMT IN	Port B input/output. Cassette tape data input.
12	PB3	In	GND (domestic) VCC (Export)	Domestic/export specification select pin
13	PB4	In	GND	User area determination pin
14	PB5	In	μPD1990C	Clock input from TP terminal of the timer IC
15	PB6	In	μPD1990C	Data input from the DATA OUT terminal of the timer IC
16	PB7	In	Key	BREAK key input (interrupt input)
17	Pφ	In	GND	PC port latch clock input
18	PC0	Out	μPD1990C	Data output to the DATA IN terminal to the timer IC
19	PC1	Out	μPD1990C	Strobe output to the STB terminal of the timer IC
20	PC2	Out	μPD1990C	Clock output to the LK terminal of the timer IC
21	PC3	Out	μPD1990C	Timer IC control signal output
22	PC4	Out	μPD1990C	Timer IC control signal output
23	PC5	Out	μPD1990C	Timer IC control signal output
24	PC6	Out	Buzzer	
25	PC7			
26	CS0	In	CPU	Chip select input connected to AD12
27	CS1	In	CPU	Chip select input connected to AD13
28	$\overline{CS2}$	In	Decoder IC	Chip select input connected to Y3 of the chip select decoder IC

I/O port (LH5810)

Pin No.	Signal Name	In/out	Connection	Functional description
29	RS0	In	CPU	Internal register and operation select signal
≀	≀	≀	≀	≀
32	RS3	In	CPU	Internal register and operation select signal
33	R/W	In	CPU	Read/write input
34	MEO	In	CPU	Memory enable and I/O port controller enable
35	ME1	In	CPU	Memory enable
36	W0	In	Option	Wait condition input
37	W1	In	Option	Wait condition input
38	GND	In	Power	0V
39	VCC	In	Power	+5V
40	DME0	Out	ROM, option	ROM enable
41	DME1	Out	Decoder	ROM enable
42	WAIT	Out	CPU	Wait signal to the CPU
43	INT	Out	CPU	Interrupt request to the CPU
44	RESET	In	RESET circuit	Initial rest signal
45	IRQ	In	Option	Interrupt request input
46	φOS	In	CPU	Basic clock input
47	CL1		CLO	Not used. Serial data reception clock input
48	SD1		(VCC)	Not used. Serial data reception input
49	LC		NC	Not used. LCD driver synchronizing signal
50	CLO	In	CL1	Serial data transmission/reception clock
51	SD0	In	CMT	Serial transmission/reception data. Use for the cassette tape data output.
52	D0	In/out	CPU	Data bus
≀	≀	≀	≀	≀
59	D7	In/out	CPU	Data bus
60	PA0	Out	Key	Port A input/output. Used as the key strobe.

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Read/write timings for I/O port
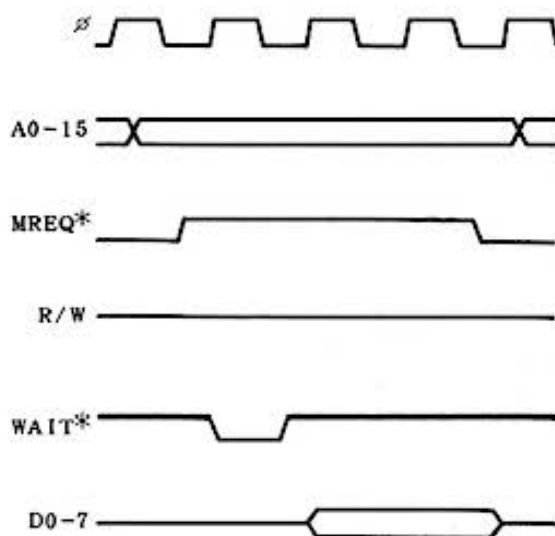
NOTE:
Clock ϕ is furnished to the ϕOS input of the I/O port. MREQ* is an inversion of $\overline{MREQ}$ of Z-80 and furnished to the ME0 of the I/O port. $\overline{WAIT}$* is an inversion of WAIT of the I/O port and furnished to the WAIT input of Z-80.
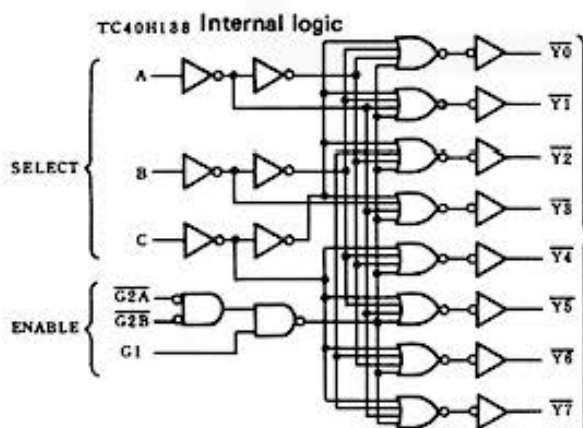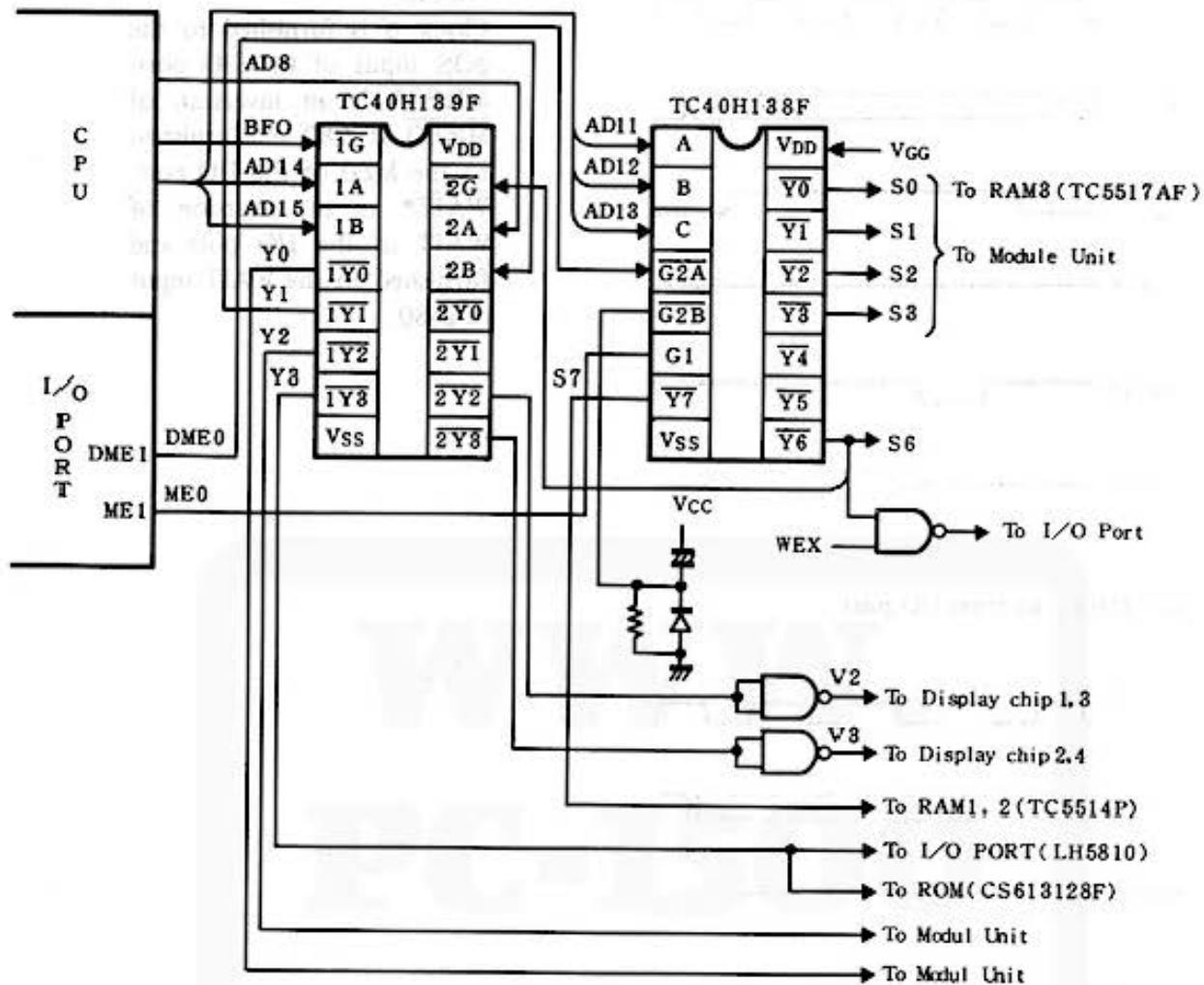
(a) Data read from I/O port
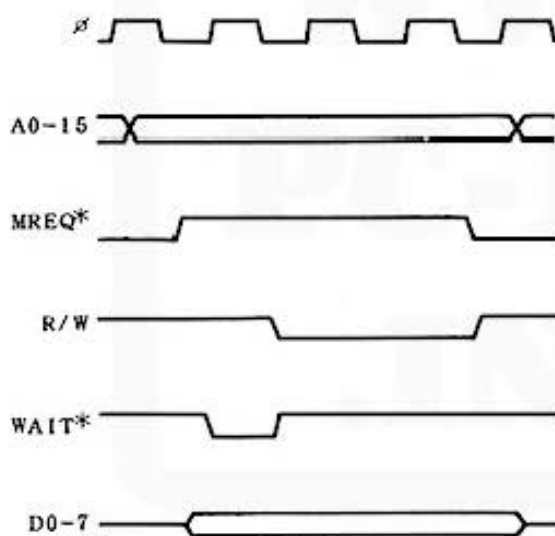
(b) Data wire to I/O port

4. CIRCUIT DESCRIPTION
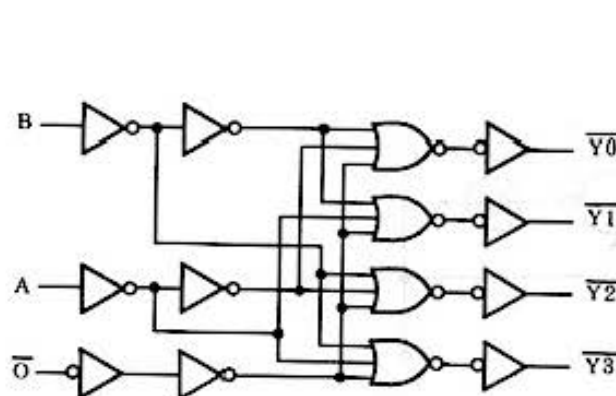
4-1. Chip Select Circuit

TC40H138 Internal logic

Truth Table

ENABLE			SELECT			Output							
01	G2A	G2B	A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	※	※	※	※	※	H	H	H	H	H	H	H	H
※	H	※	※	※	※	H	H	H	H	H	H	H	H
※	※	H	※	※	※	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

※ : Dodt care

Truth Table

Input			Output			
ENABLE	SELECT					
$\bar{G}$	A	B	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	※	※	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

※= Irrelevant

- Selection of $\overline{1Y0} \sim \overline{1Y3}$ by the decoder IC (TC40H139H) is done when the gate signal $(\overline{GI})$ input BF0 is low.

  $\underline{Y0}$ With low state of AD14 and AD15, the Y0 output becomes low to select the system
  $(\overline{1Y0})$ ROM area of the module unit. (0000 ~ 3FFF address setup)

  $\underline{Y1}$ With high state of AD14 and low state of AD15, the Y1 output becomes low to select
  $(\overline{1Y1})$ the gate $(\overline{G2A})$ of the IC (TC40H138F). (4000 ~ 7FFF address setup)

  $\underline{Y2}$ With low state of AD14 and high state of AD15, the Y2 output becomes low to select
  $(\overline{1Y2})$ the expansion ROM area of the module unit. (8000 ~ BFFF address setup)

  $\underline{Y3}$ With high state of AD14 and AD15, the Y3 output becomes low to select the system
  $(\overline{1Y3})$ program ROM (CS-613128F) and the I/O port (LH5811). (C000 ~ FFFF address setup)

- Selection of S0 ~ S7 by the decoder IC (TC40H138F) is done when the gate signal input ME0 (G1) is high, Y1 $(\overline{G2})$ low, and $\overline{G2B}$ is low (which is normally low).

  $\underline{S0}$ With all of AD11, AD12, and AD13 in low state, S0 goes to the low state and selects the
  $(\overline{Y0})$ RAM3 (TC5517AF). (4000 ~ 47FF address setup)

  $\underline{S1}$ With high state of AD11 and low state of AD12 and AD13, S1 goes to the low state to
  $(\overline{Y1})$ select the option user RAM area. (4800 ~ 49FF address setup)

  $\underline{S2}$ With low state of AD11 and high state of AD12 and low state of AD13, S2 goes to the
  $(\overline{Y2})$ low state to select the option RAM area. (5000 ~ 57FF address setup)

  $\underline{S3}$ With high state of AD11 and AD12 and low state of AD13, S3 goes to the low state to
  $(\overline{Y3})$ select the option user RAM area. (6000 ~ 67FF address setup)

  $\underline{S6}$ With low state of AD11 and high state of AD12 and AD13, S6 goes to the low state to
  $(\overline{Y6})$ receive the interrupt input from an option into the I/O port. (7000 ~ 77FF address setup)

  $\underline{S7}$ With all of AD11, AD12, and AD13 in high state, S7 goes to the low state to select the
  $(\overline{Y7})$ system memory RAM1 and 2 (TC5514P). (7800 ~ 7FFF addres setup) RAM1 and RAM2 are 4-bit RAMs, independently used to assume low order and high order bits to comprise one byte with a pair of 4 bits each.

- Selection of $\overline{2Y2}$ and $\overline{2Y3}$ by the decoder IC (TC40H139) is done when the gate of $\overline{2G}$ becomes active with the selection of the TC40H138F output, S6 $(\overline{Y6})$.

  $\overline{2Y2}$ With low state of AD8 and high state of DME0, the $\overline{2Y2}$ output goes to the low state so
  (V2)   that the NAND gate output V2 is turned high to select the display chip 1 and 3.

  $\overline{2Y3}$ With high state of AD8 and DME0, the $\overline{2Y3}$ output goes to the low state so that the
 (V3)   NAND gate out V3 is turned high to select the display chip 2 and 4.

* Display chip (SC882G) is a 4-bit RAM, comprised of one byte of data with 4 low order bits and 4 high order bits of data, so that even the chip select signals are used in pair of chip 1 with chip 3 and chip 2 with chip 4.

15
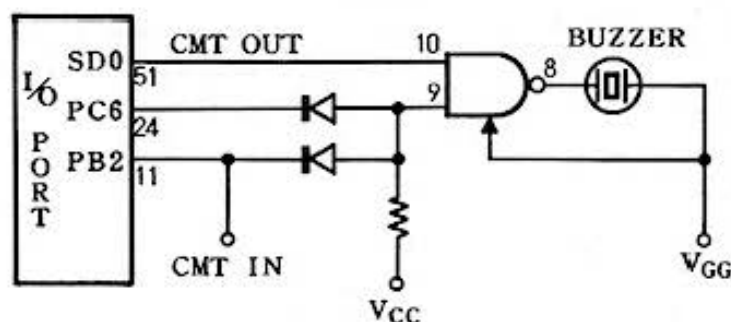
2) Buzzer circuit

The control signal CMT OUT is setnt out from the pin SD0 of the I/O port wich sounds the buzzer in combination with the low state of either the programmed output from the I/O port or CMT IN sent from the cassette tape deck.

3) RAM R/W signal circuit
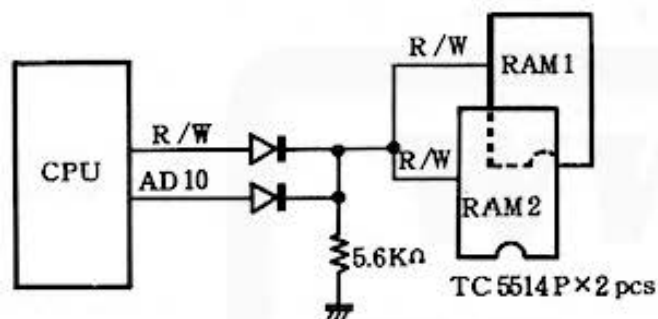
This circuit prevents writing if AD10 is in high state during the write mode (when R/W is low). This is to prevent wrong operation when a specific key, ↓ or ↑ is pushed without performing "NEW 0 ENTER" after battery replacement.

4) ON key double action preventive circuit
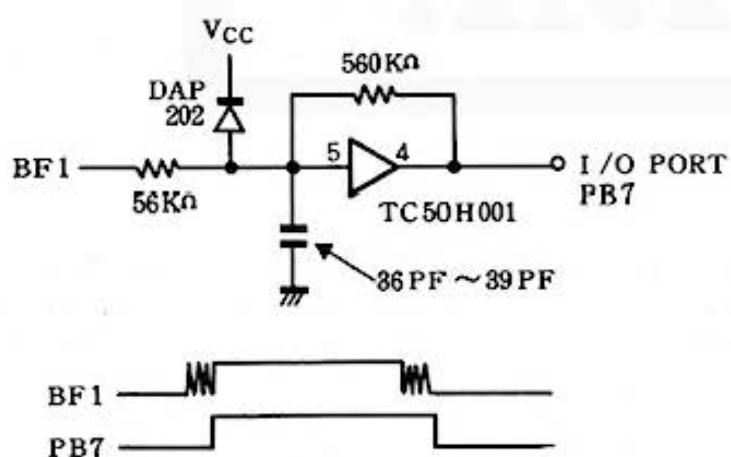
This circuit consists of the Schmitt circuit that prevents the possibility of setting the input flag of the LH5811 I/O port which depends on how the ON key is pushed.

5) Timer/counter circuit

82.768KHz
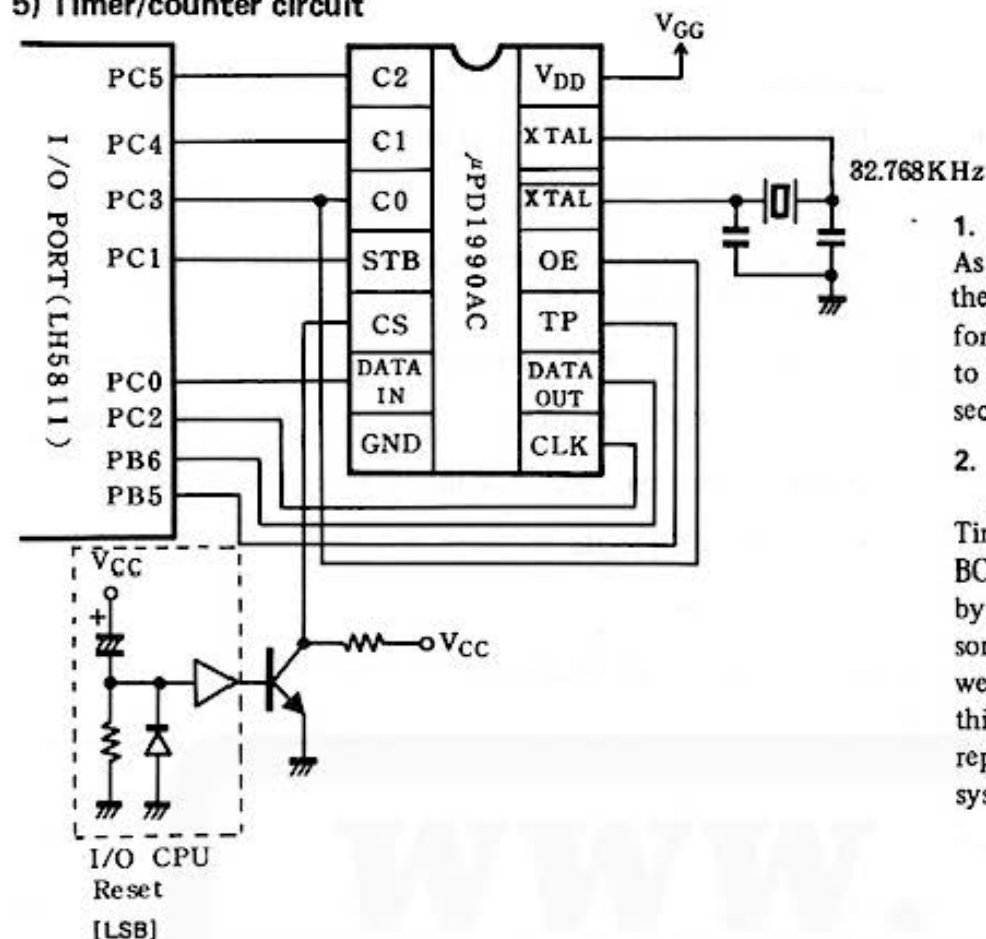
1. Outline

As shown in the left, the μPD1990AC is used for the time keeping IC to count hour/minute/ second/month/day.

2. Main function of μPD1990AC

Time data is in the BCD form and is judged by means of comparison. However, day of week is not used with this chip and hour is represented by 24-hour system.

[LSB]   [MSB]

9	4	3	2	1	2	5	2	✕	B
Seconds		Minutes		Hours		Day		Week	Month
4	4	4	4	4	4	4	4	4	4
Bits	Bits	Bits	Bits	Bits	Bits	Bits	Bits	Bits	Bits

D OUT ←   D IN ←
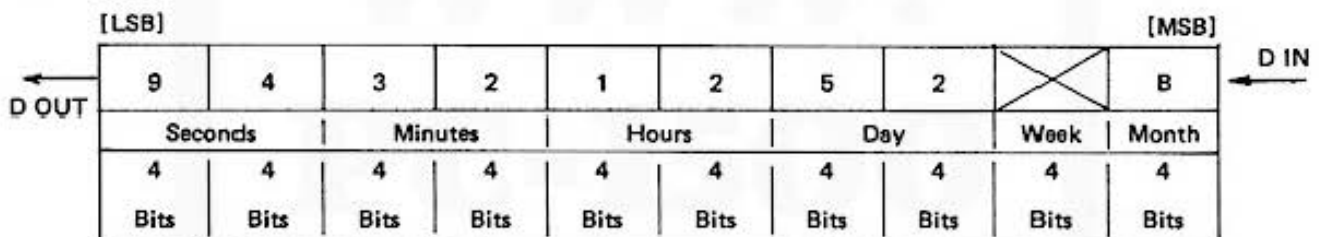
Pin No.	Signal name	In/out	Description
1	C2	In	Mode select signal
2	C1	In	Mode select signal
3	C0	In	Mode select signal
4	STB	In	Strobe. Command is latched by the strobe STB.
5	CS	In	Chip select: disables CLK and STB input and DATA OUT output by the CS input. All input/output are invalid unless CS is high.

			C2=0	
C1	C0	Mode	Data In/out mode
0	0	0	Resister hold
0	1	1	Registered shift
1	0	2	Time set
1	1	3	Time read

STB
CS   Internal STB (command latch clock)

CLK   Internal CLK (40-bit serial clock)

OE   Internal OE (gate input of DAT OUT)

17

6	DATA IN	In	Data input signal (40-bit serial data)
7	GND	In	0V
8	CLK	In	40-bit shift register clock (Data input/output is carried out in synchronization with CLK.
9	DATA OUT	Out	Data output signal (40-bit serial data)
10	TP	Out	Timer pulse output: to C0, C1, C2 during command assignment.
11	OUT ENABLE	In	Output enable: input to control the output of DATA OUT.
12	$\overline{XTAL}$	In	Basic clock, 32.768KHz
13	XTAL	In	Same the above
14	VDD	In	Source power input, connected to VGG (4.7V).

6) Power supply circuit

The power supply is incorporated in a single resin molded IC that consists of the stabilizer circuit, temperature compensation circuit, and bleeder circuit.
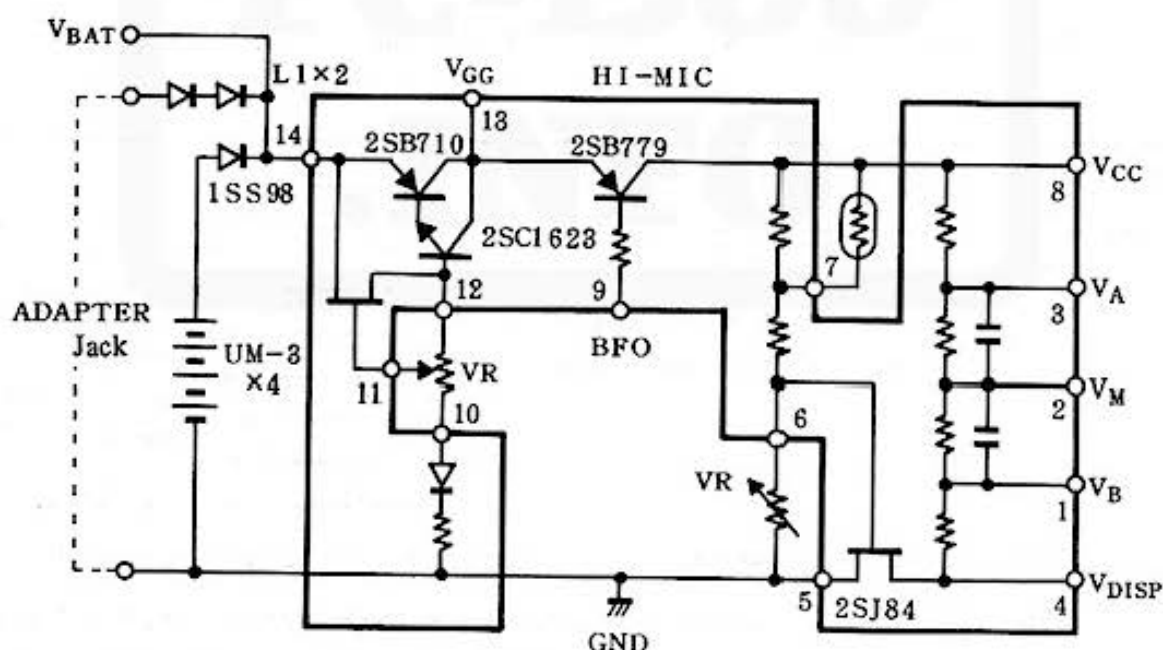

Supply voltage: 1.5V x 4 = 7V ±0.05V
VGG: 4.7V
VCC: 4.7V ±0.02V
VDISP: 3.7V ±0.01V
(In the case of 25°C)

5. STERVICING

1) Measures against irregular condition

In a rare case, all keys on the keyboard might become inoperative, including the $\boxed{\text{ON}}$ BREAK key, when a strong external noise interference is met or when a strong impact is given to the machine body. When such a condition is encountered, keep the ALL RESET key pushed for a period of about 15 seconds while depressing the $\boxed{\substack{\text{BREAK}\\\text{ON}}}$ key.

Depressing $\boxed{\text{ON}}$ BREAK key.
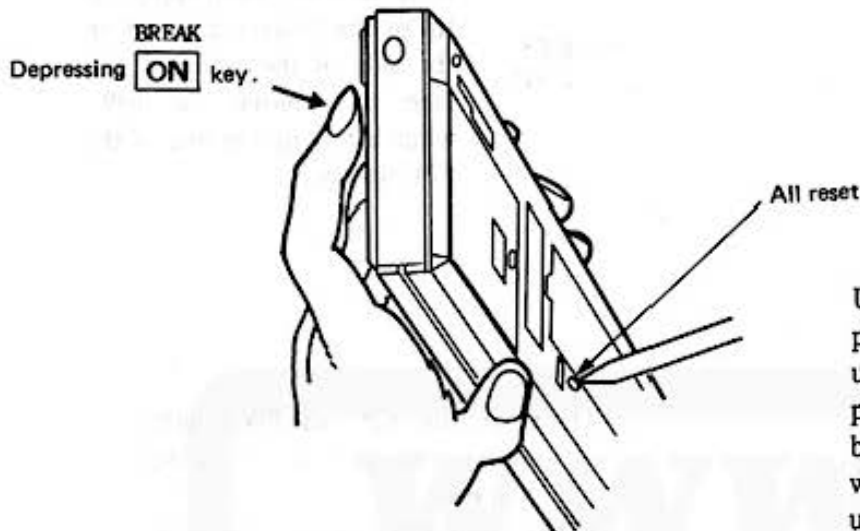
All reset

Use the tip of a ball point pen to push the ALL RESET SW. Do not use the tip of something such as a pencial of which the tip is liable to break. Also, do not use anything with a sharp edge such as a needle up.

Wait for the prompt $\boxed{\text{"NEW 0?: CHECK"}}$ to appear on the display, then push $\boxed{\text{CL}}$ NEW 0 $\boxed{\text{ENTER}}$.

If the prompt "NEW 0?: CHECK" does not appear, try the above entry again.

Do not use the ALL RESET switch except for the above operation, or destruction of the program, data, and reserve contents will occur.

2) How to replace FPC (Flexible Printed Cable)

To replace the FPC that connects the Key PWB with the Operation PWB, the following procedure should be used.

2-1. Removal

Saldering

Key PWB

FPC

Machine PWB
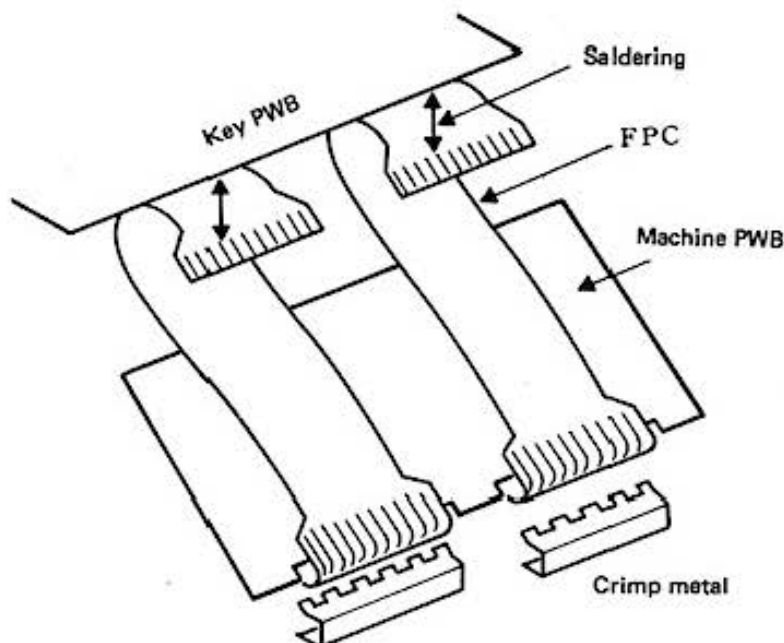
Crimp metal

Since the Operation PWB is connected with the FPC by means of the crip metal, the Key PWB is disconnected from the Operation PWB after removing the crimp metal.
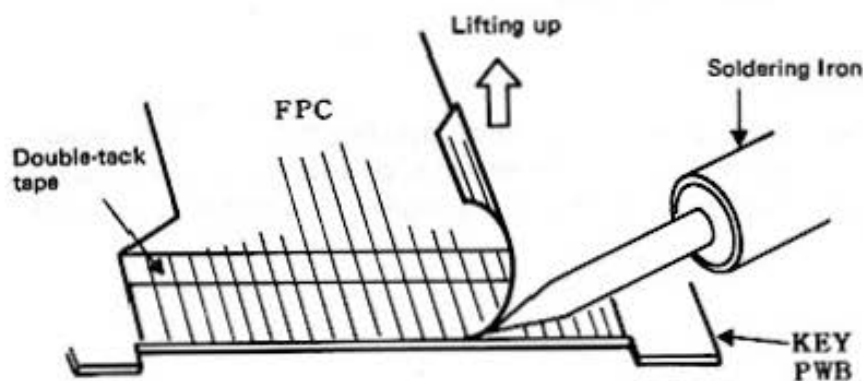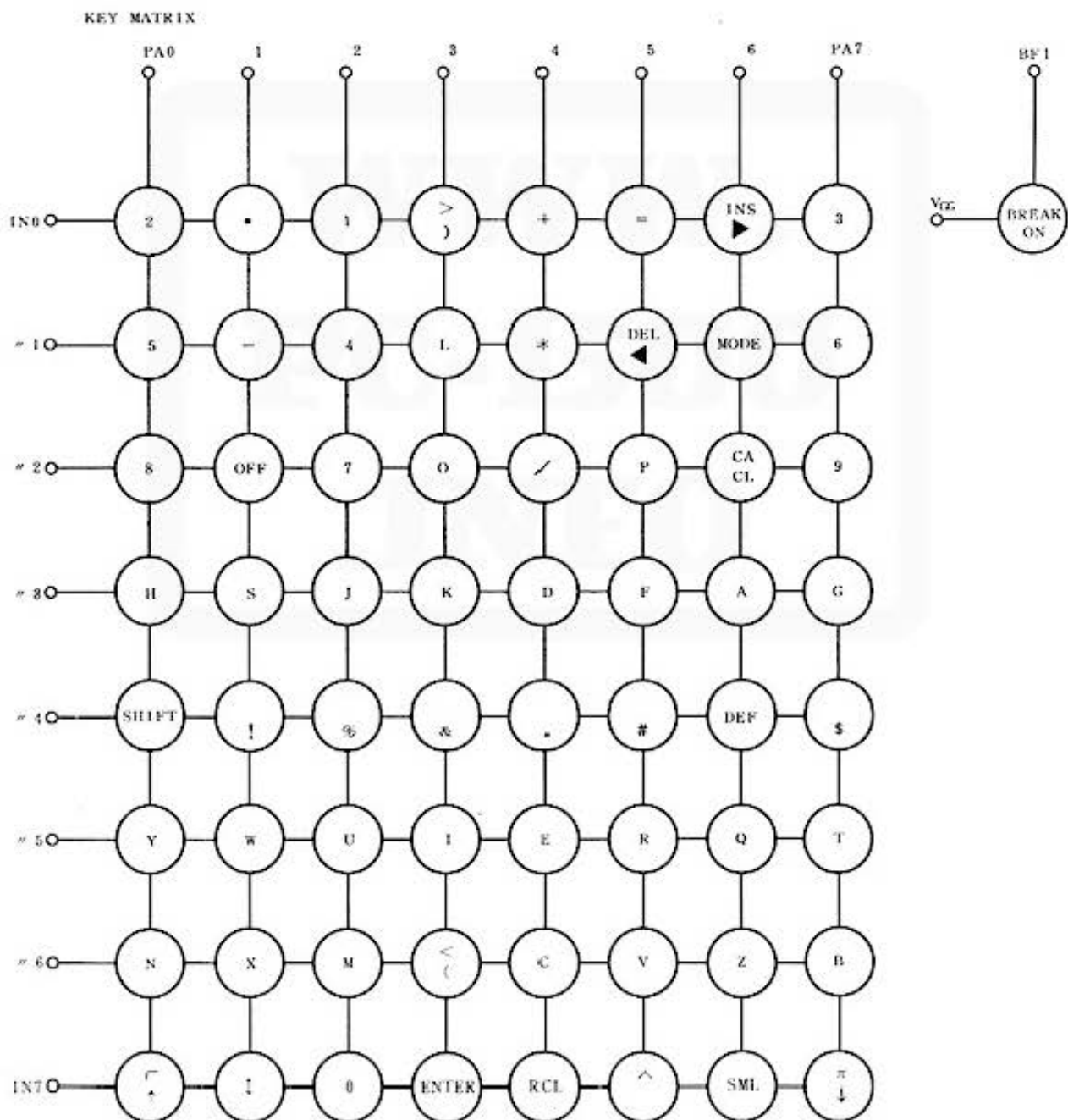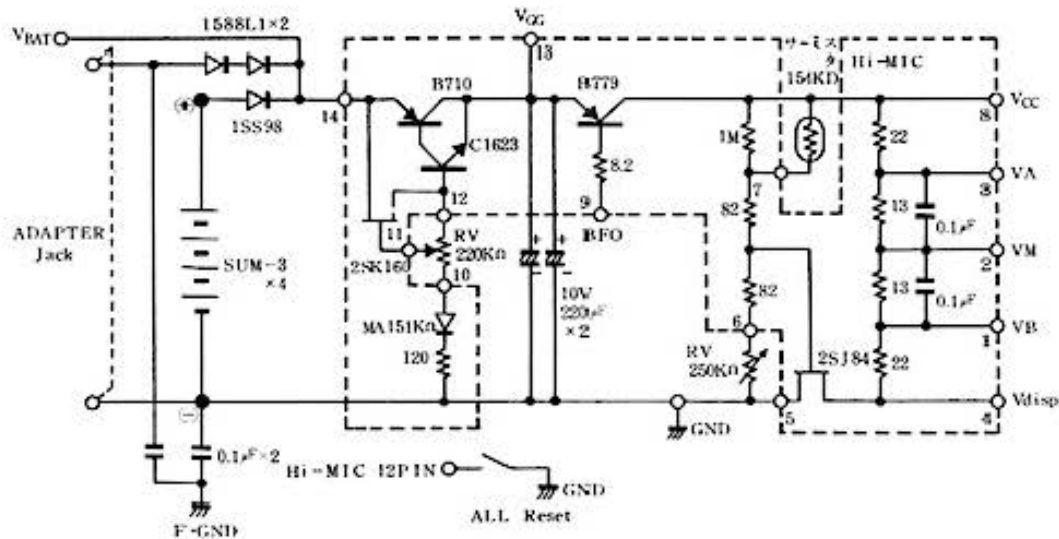
The Key PWB is connected with the FPC by soldering. Peel away the double-tack tape that fastens the FPC with the PWB, then apply the tip of the soldering pencil on the side of the soldered surface to remove the FPC, while lifting up the end of the FPC lightly.
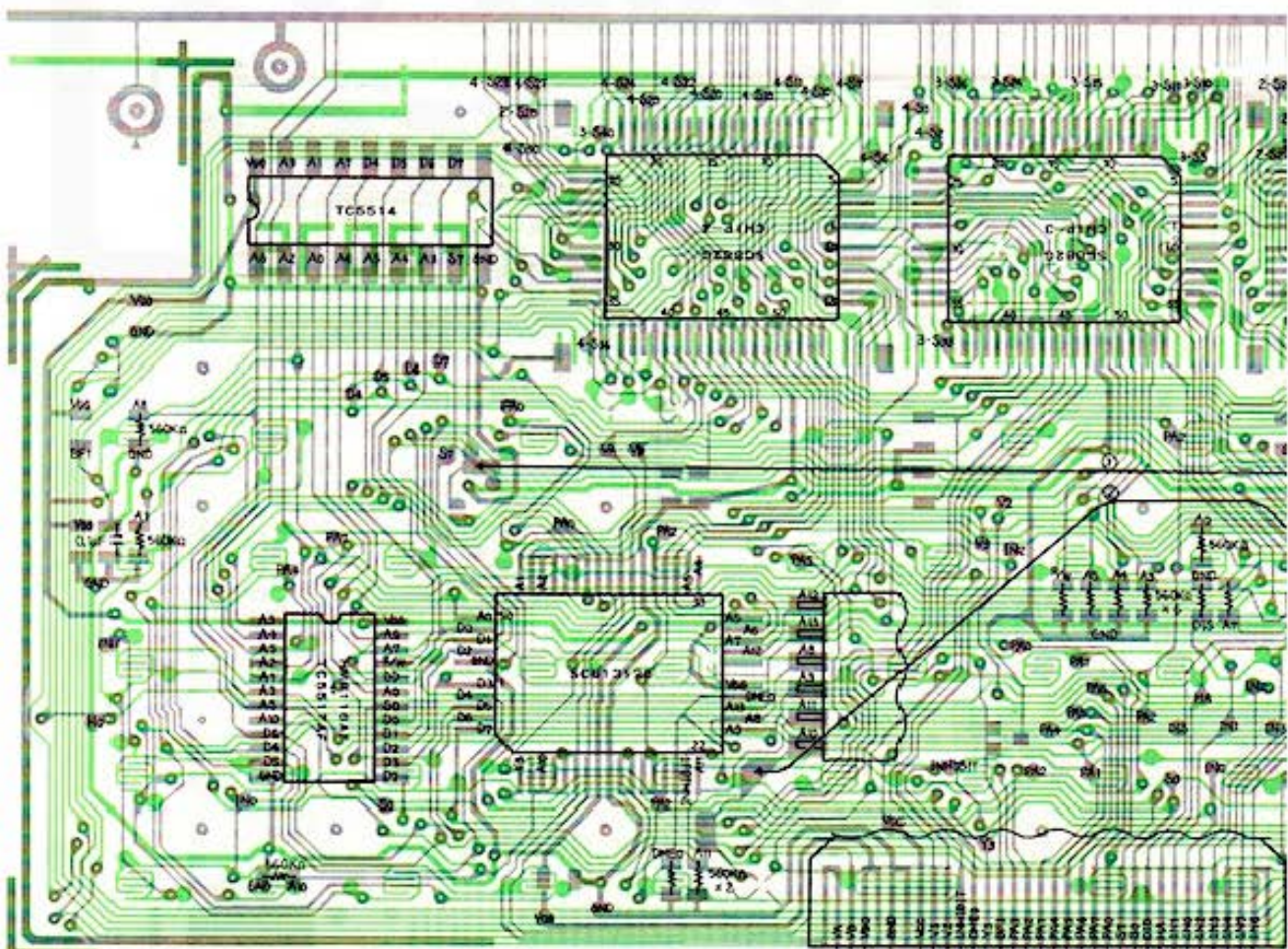
2-2. Replacing
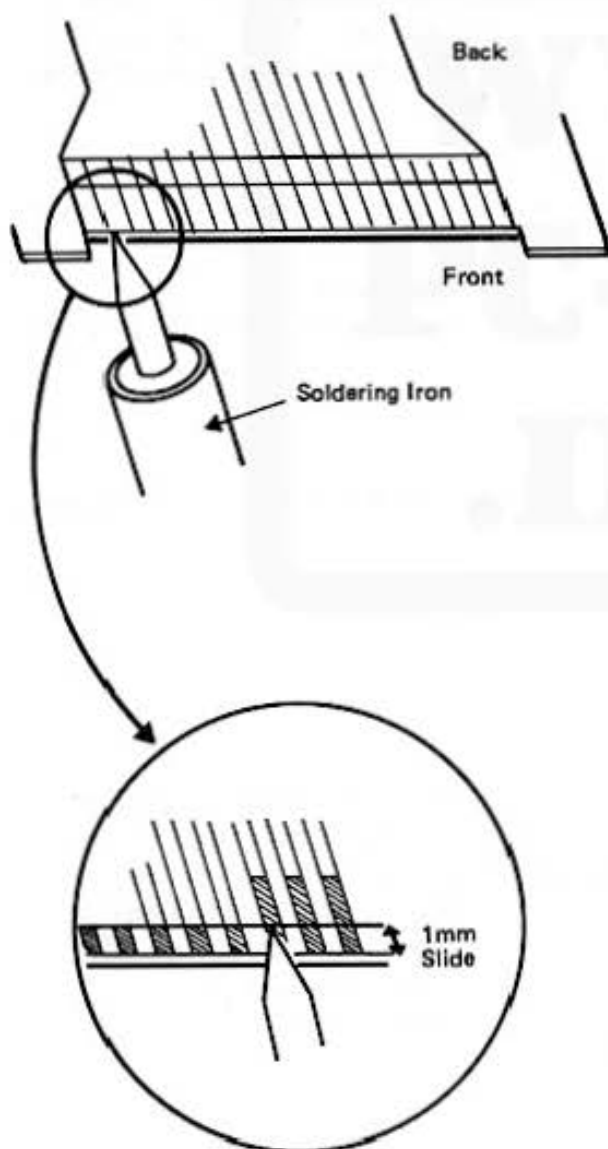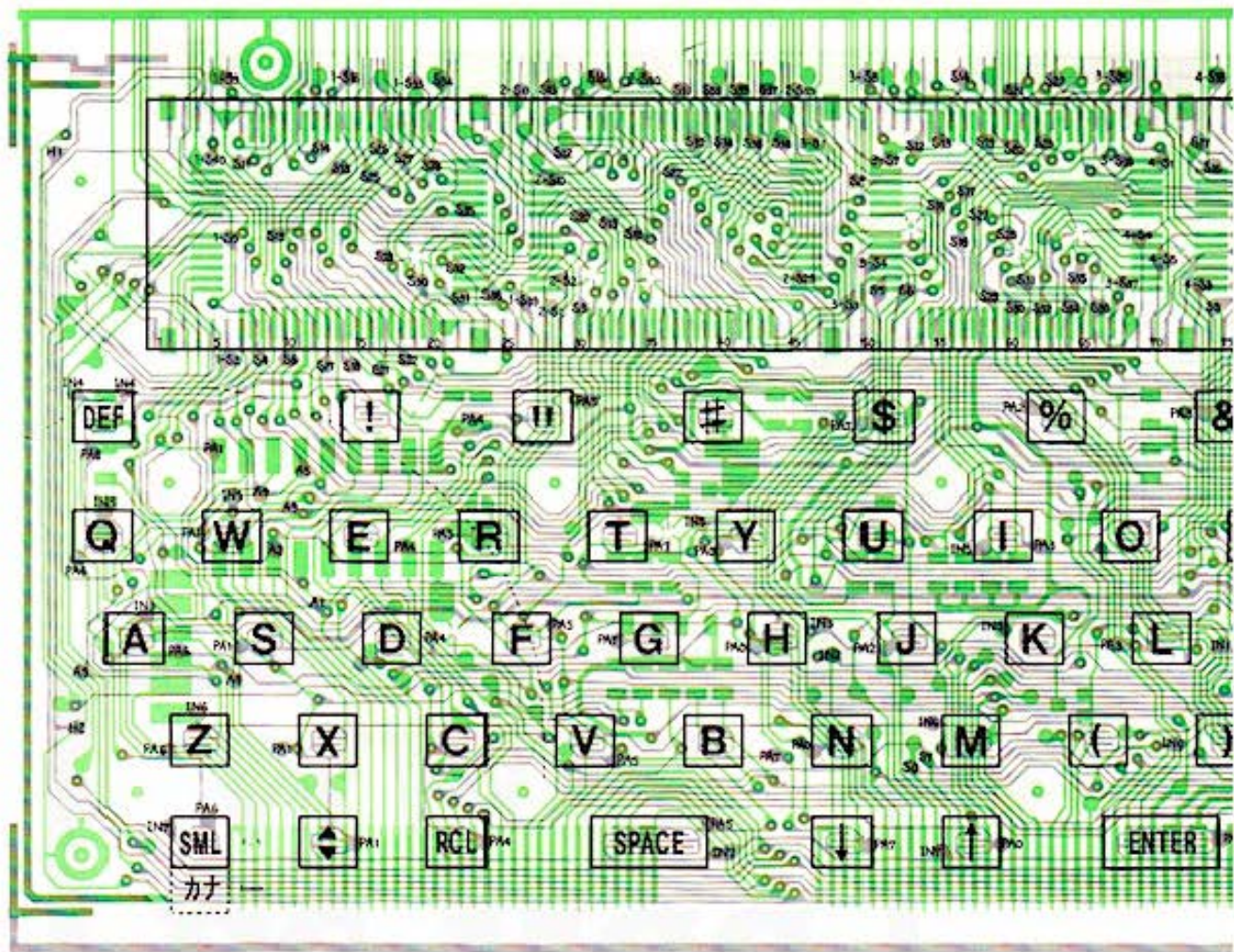

(1) Coat the FPC ad PWB with solder with care not to make it uneven.

(2) Temporarily secure the FPC using the double-tack tape.

(3) Match the printed circuit pattern of the PWB with FPC and secure them temporarily. Slide the FPC about 1mm backward in this case.

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6. PC-1500 KEY & POWER SUPPLY CIRCUIT

KEY MATRIX

21

Production)

2 Production)

ADAPTER
JACK

→ Battery ⊕

→ Battery ⊖

RV250KΩ

RV220KΩ

H - MIC

LH-5810

40 PIN
CONNECTOR

INHIBIT

RESET Terminal
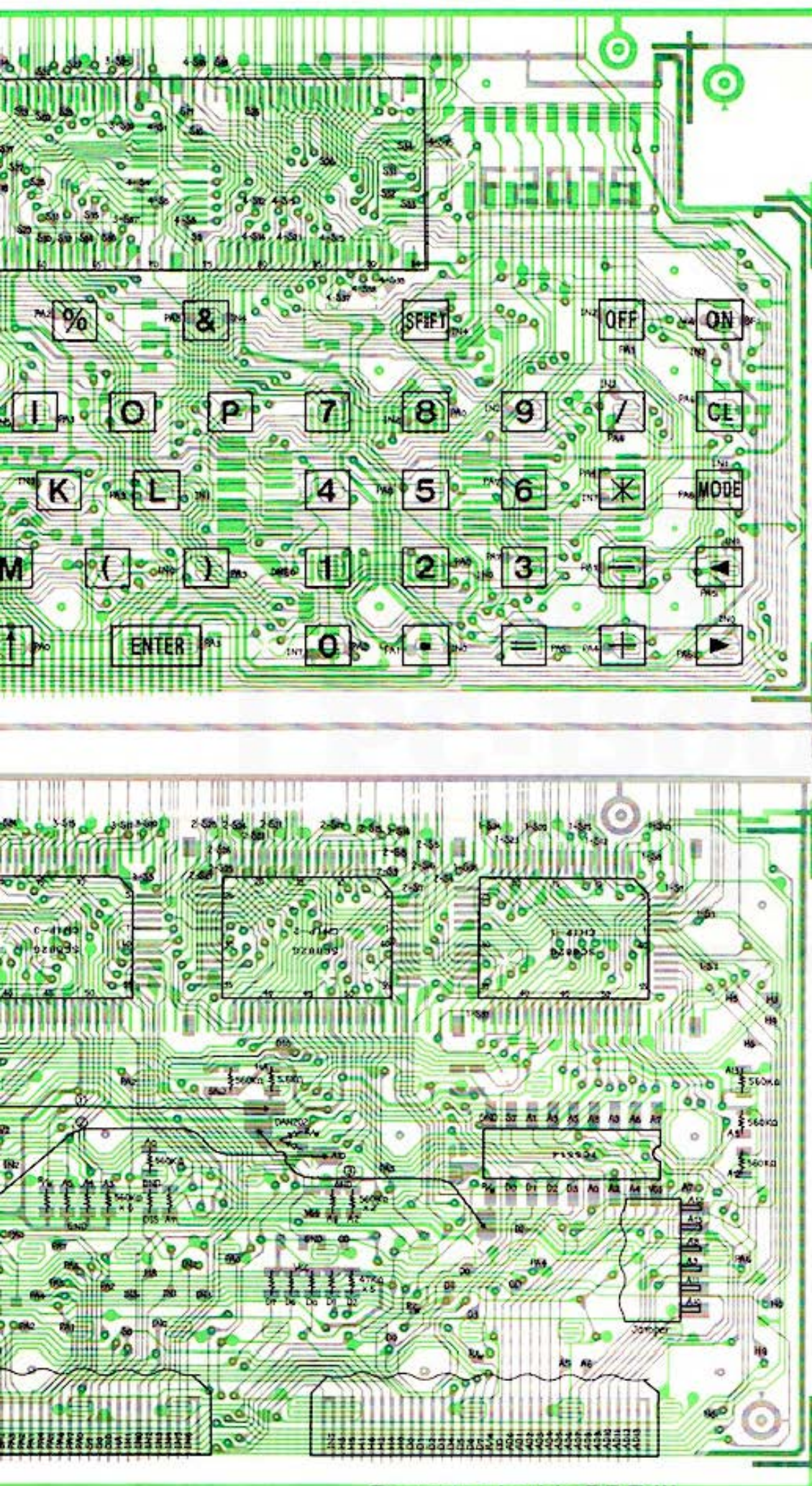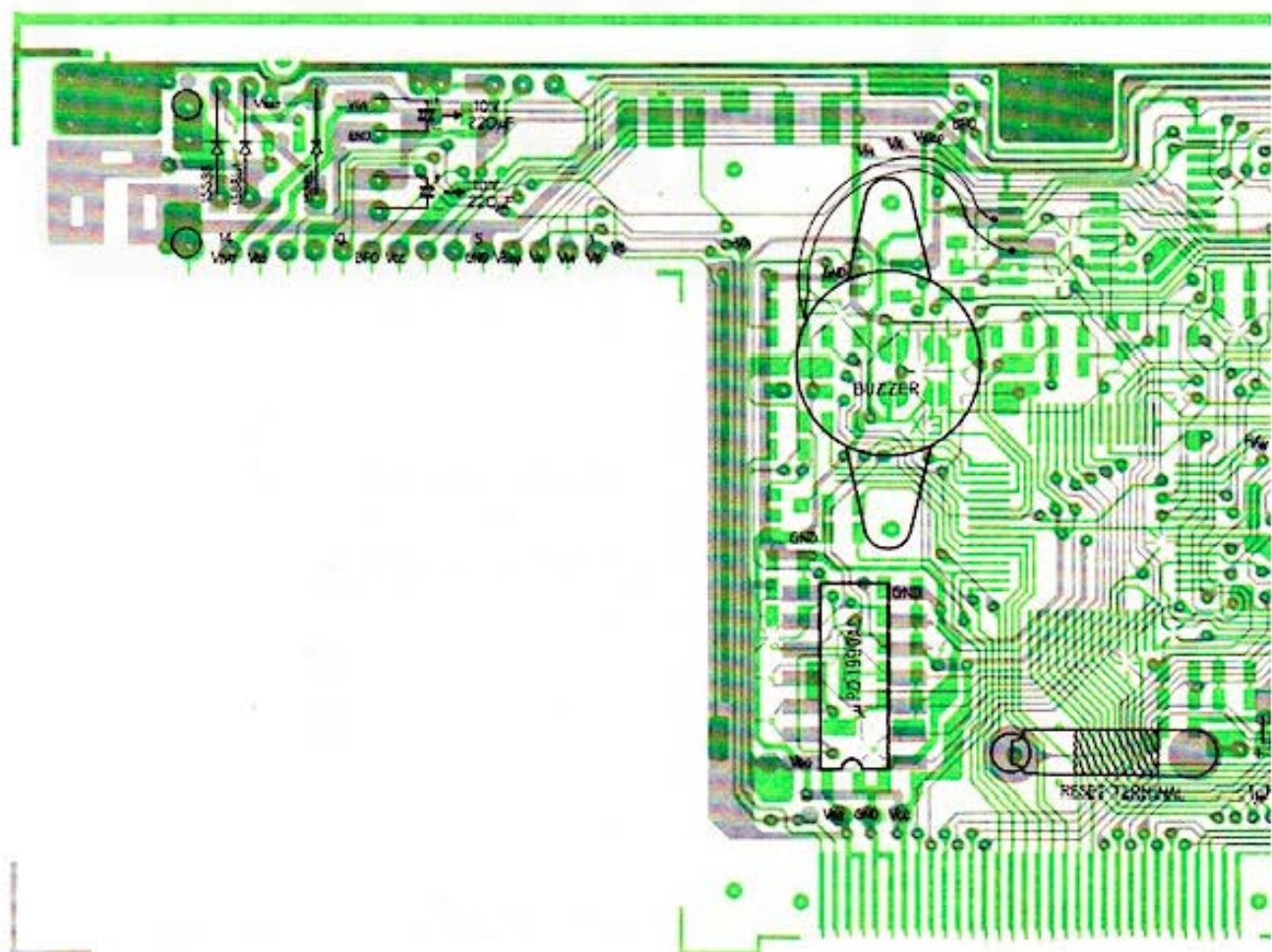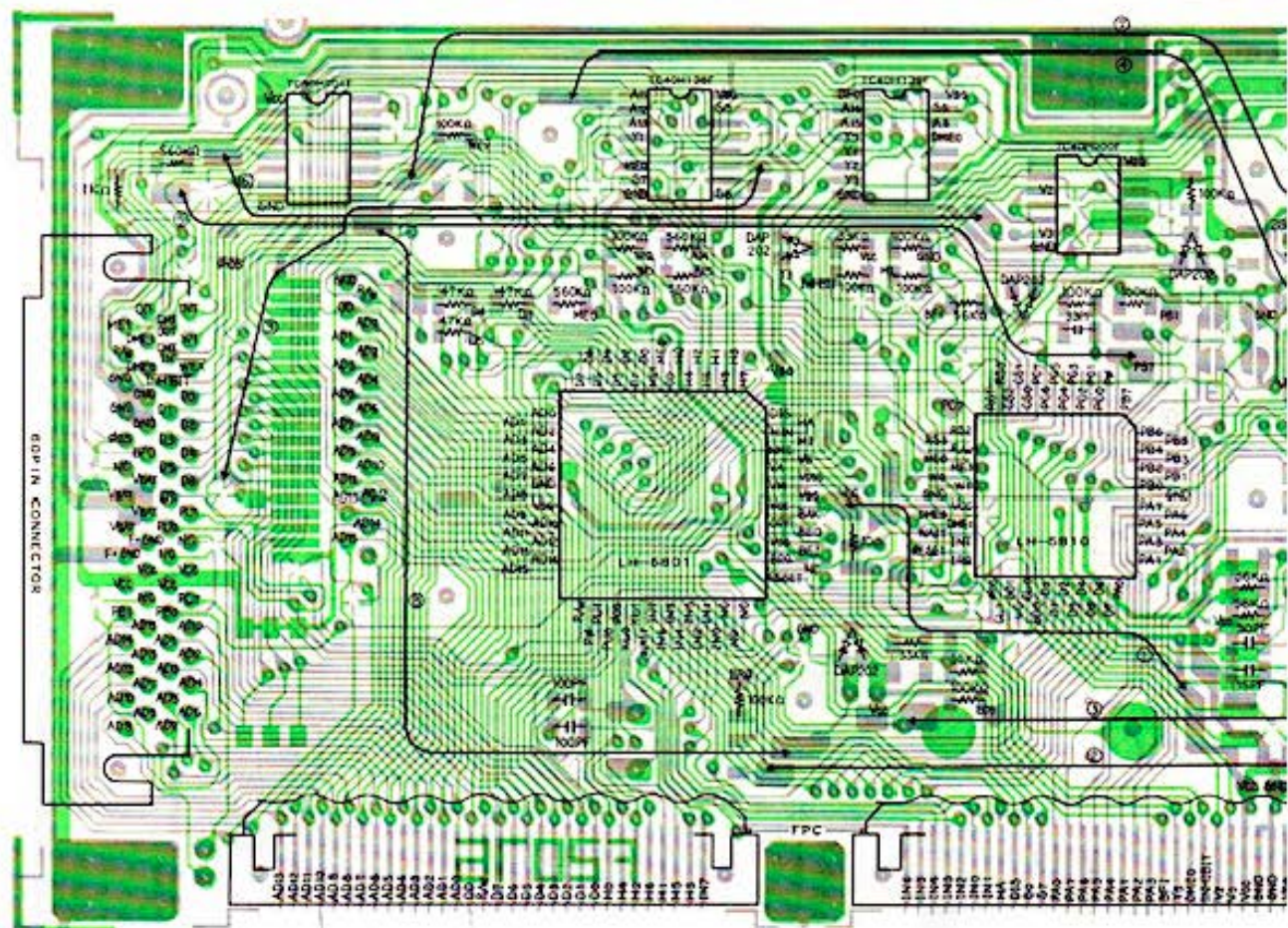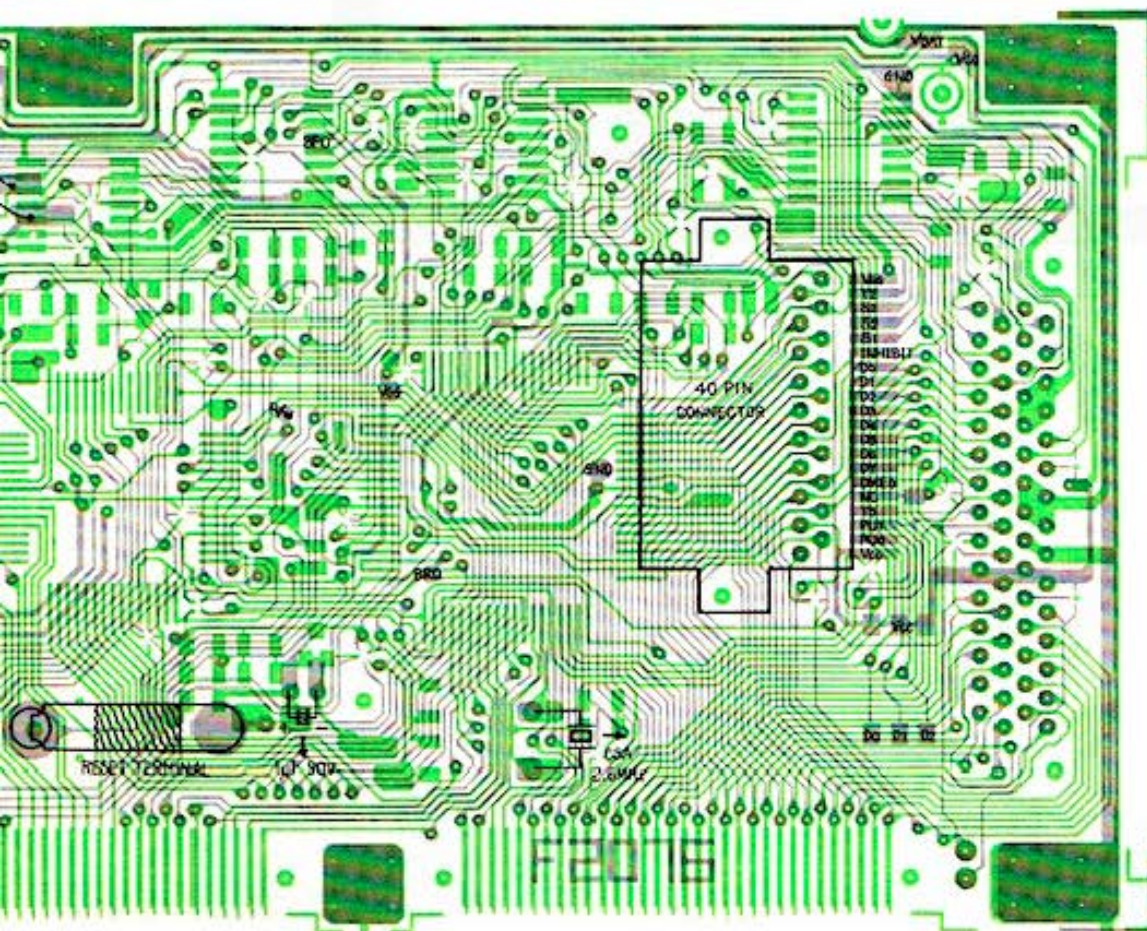
PC-1500 MAIN P.W.B (1982年7月生産より)
PC-1500 MAIN P.W.B (From the July 1982 Production)

RV220KΩ

MA-1066

0.1μF

ADAPTER
JACK

→ Battery ⊕

→ Battery ⊖

40 PIN
CONNECTOR

Vdd
Y1
S3
S2
S1
INHIBIT
D0
D1
D2
D3
D4
D5
D6
D7
DME0
NC
Y0
PU1
PU0
Vcc

Ceramic oscillator
CSA 2.6MHz

1μF 50V
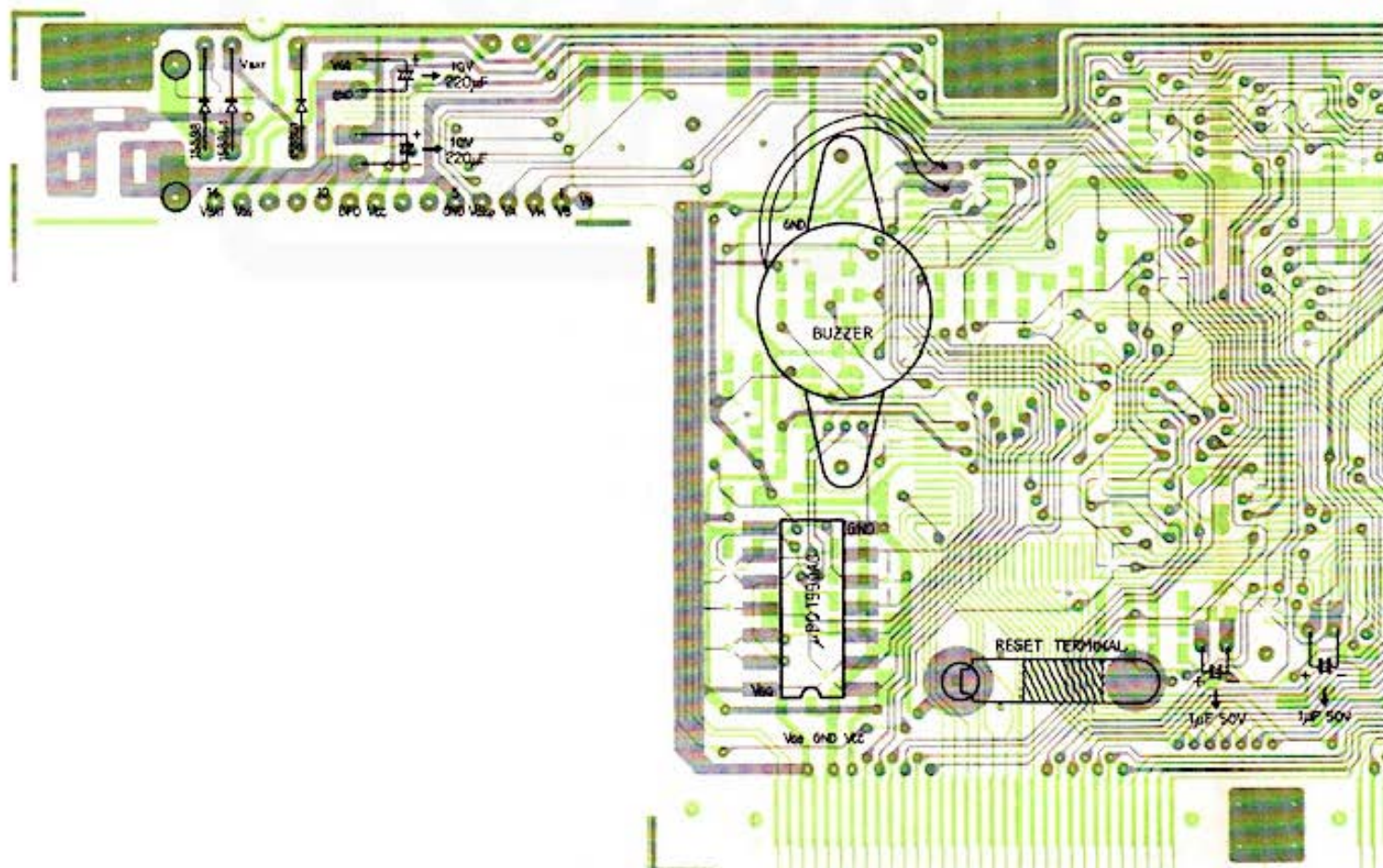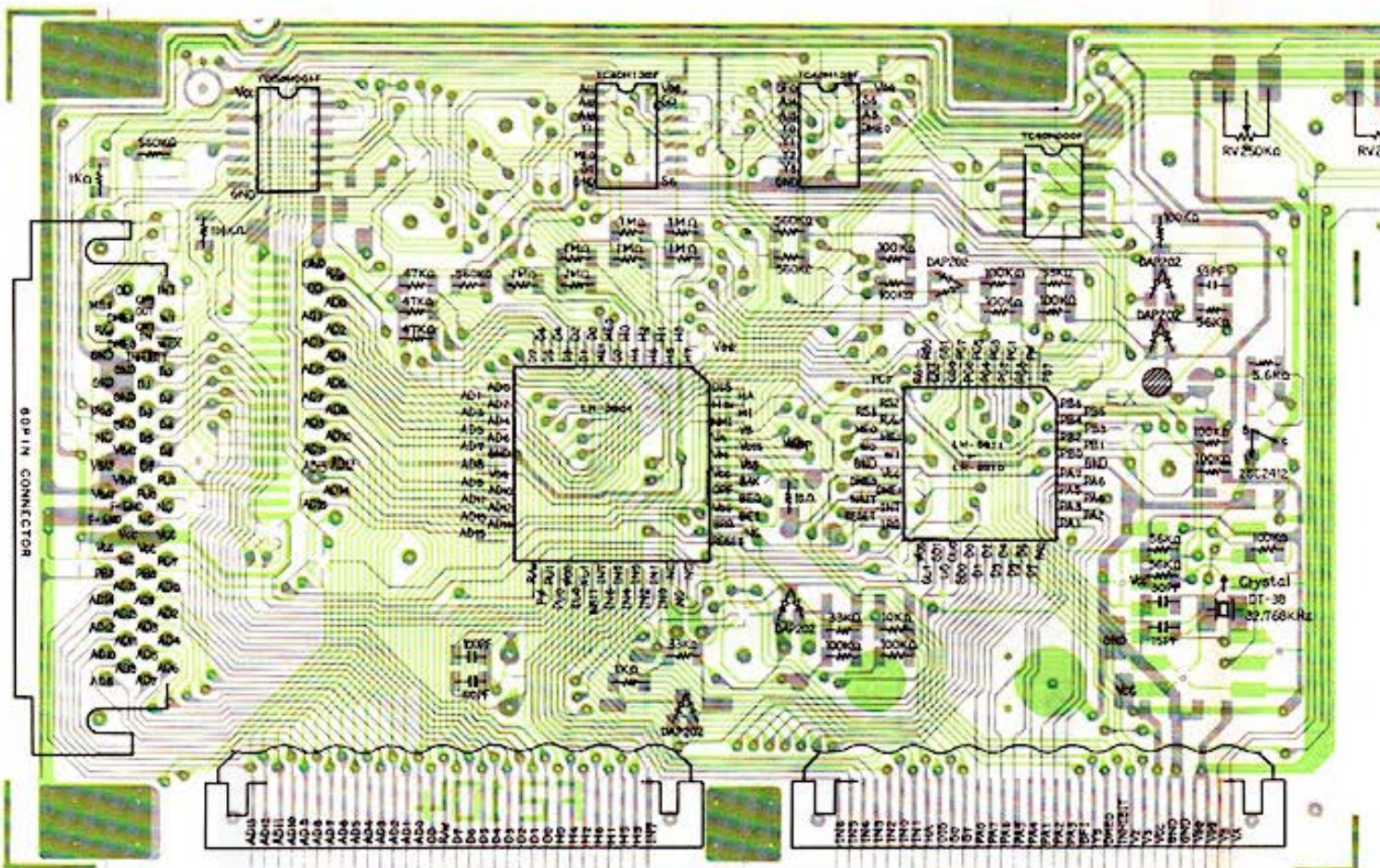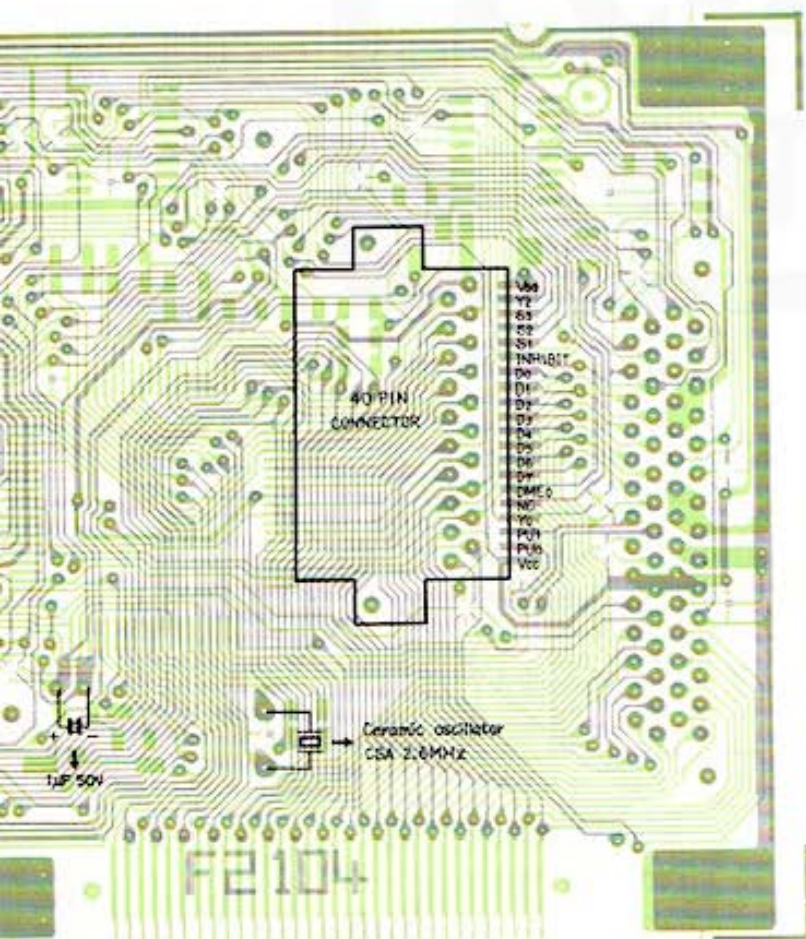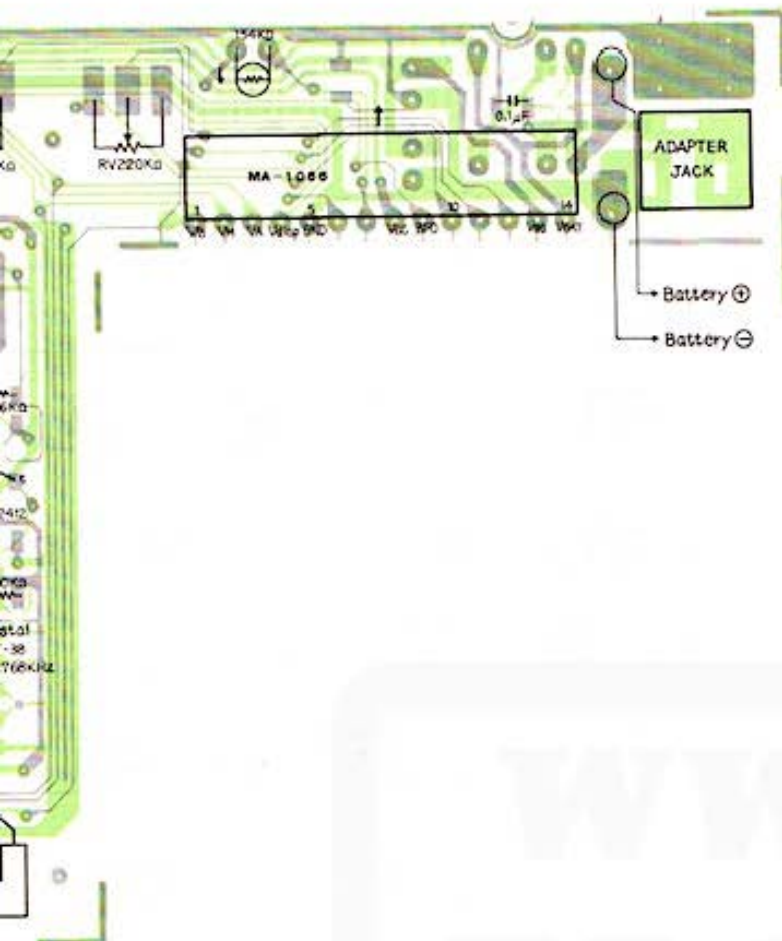
10. LCD SEGMENT & BACK-PLATE SIGNAL
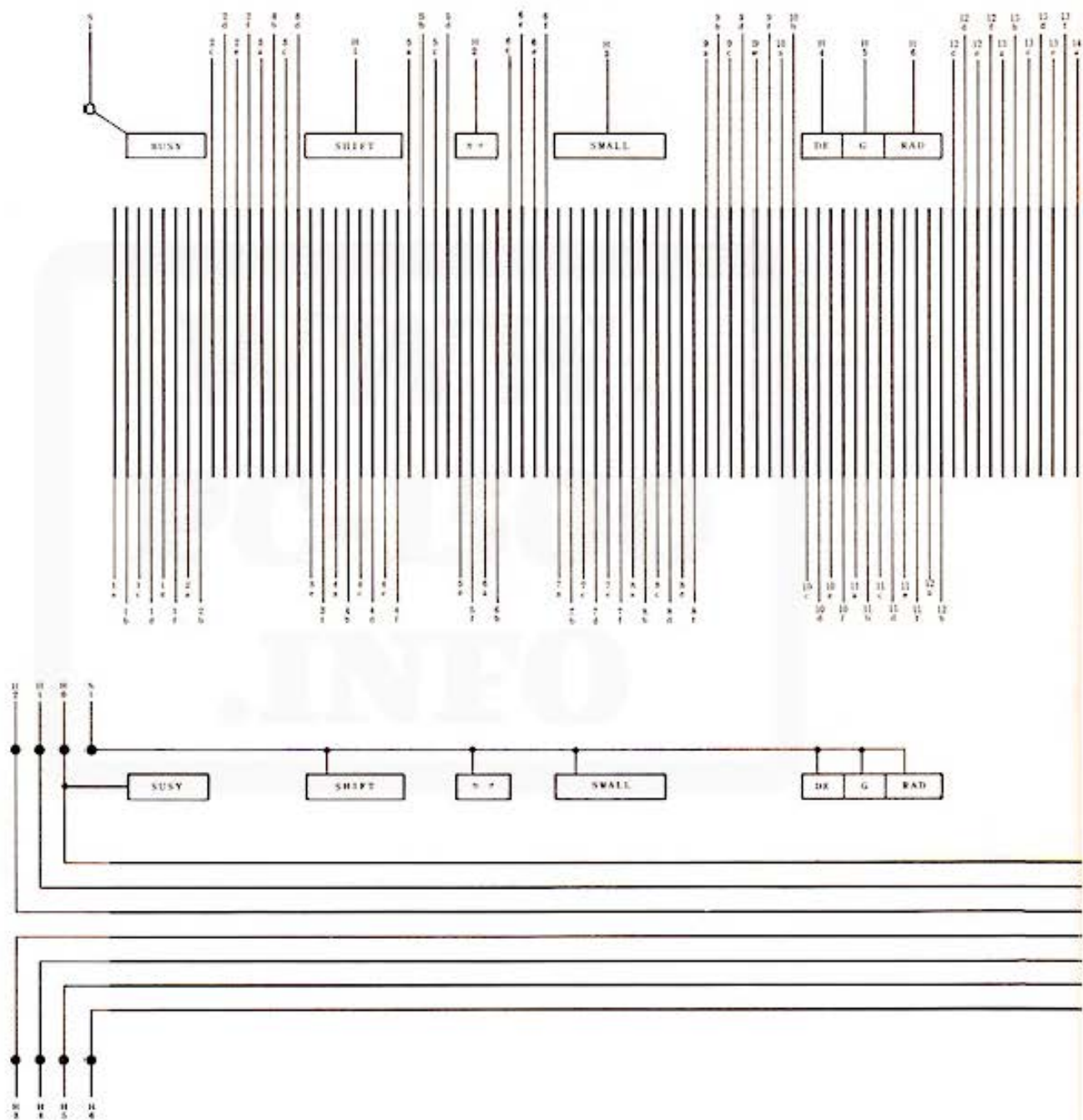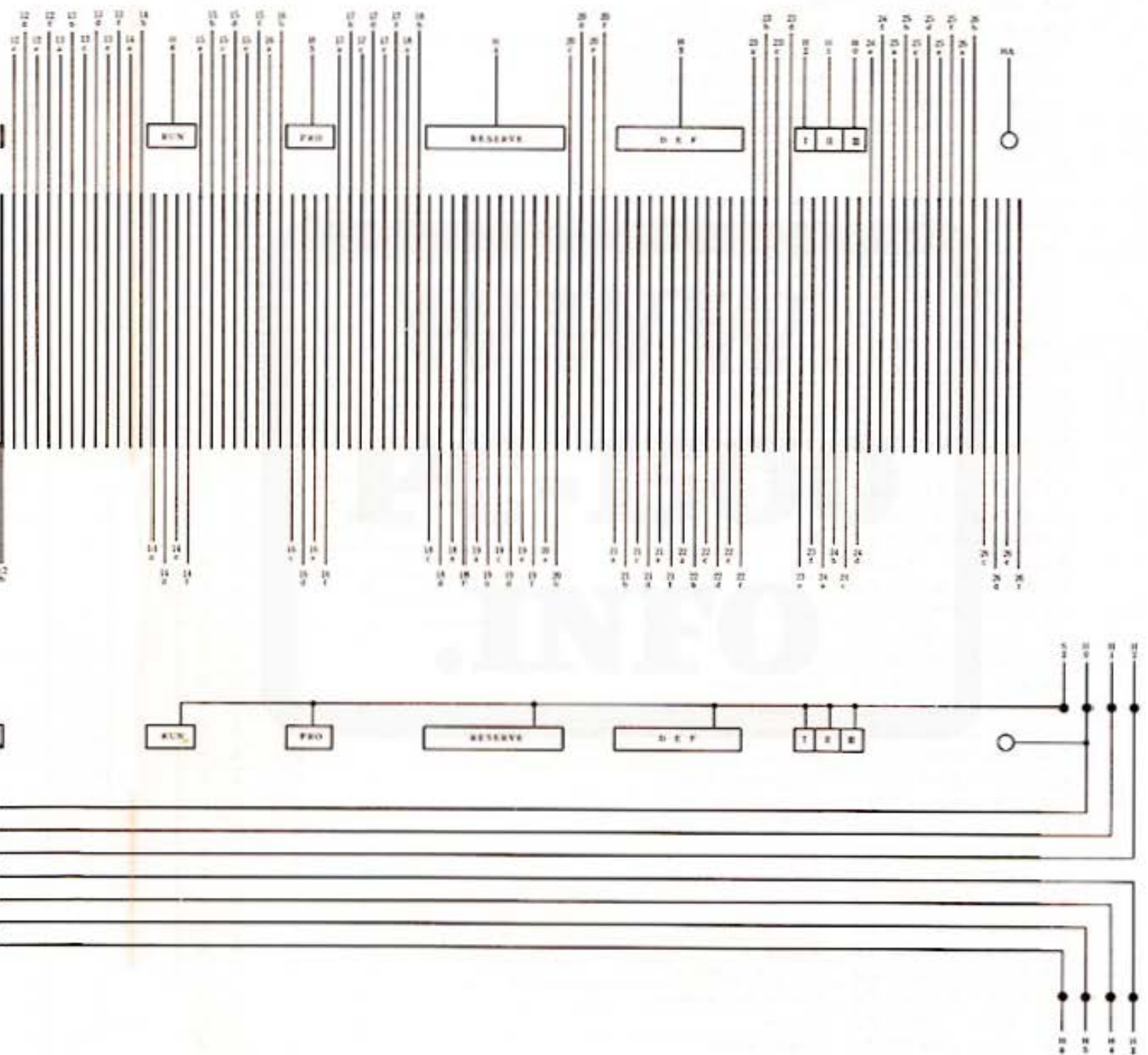
11. PARTS LIST & GUIDE

NO.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK	
1	LX—BZ1123CCZZ	Screw	N	C	A	A
2	DUNTG6449CCZZ	Cabinet top unit	N	D	A	S
3	GFTAA1267CCZZ	Connector lid	N	D	A	C
4	PFiLW1391CCZZ	Display filter	N	C	A	D
5	PSLDP1322CCZZ	Display mask	N	C	A	C
6	PFiLW1354CCZZ	Polarization filter	N	C	A	E
7	LANGK1437CCZZ	Angle for LCD	N	C	A	C
8	PTPEH1033CCZZ	LCD fixing tape		C	A	A
9	VVLLF8082GE—1	LCD	N	B	B	A
10	PGUMS1190CCZZ	Rubber connector		B	A	F
11- 1	JKNBZ1731CC01	Keytop 1set/each 1PC	N	C	A	G
11- 2	JKNBZ1733CC01	Key top 1set/10PCS	N	C	A	F
11- 3	JKNBZ1705CC05	Key top 1set/each 1PC	N	C	A	F
11- 4	JKNBZ1705CC10	Key top 1set/20PCS	N	C	A	F
11- 5	JKNBZ1705CC06	Key top 1set/20PCS	N	C	A	F
11- 6	JKNBZ1705CC07	Key top 1set/20PCS	N	C	A	F
11- 7	JKNBZ1705CC08	Key top 1set/10PCS	N	C	A	F
11- 8	JKNBZ1732CC01	Key top 1set/10PCS	N	C	A	F
11- 9	JKNBZ1622CC01	Key top 1set/20PCS	N	C	A	E
11-10	JKNBZ1515CC10	Key top 1set/20PCS	N	C	A	F
11-11	JKNBZ1495CCZZ	Key top 1set/30PCS	N	C	A	D
11-12	JKNBZ1515CC11	Key top 1set/20PCS	N	C	A	F
11-13	JKNBZ1515CC12	Key top 1set/20PCS	N	C	A	F
11-14	JKNBZ1493CC03	Key top 1set/30PCS	N	C	A	E
12	PGUMM1389CCZZ	Key rubber	N	C	A	L
13	DUNTK6381CCZZ	Key PWB unit	N	E	C	A
14	LX—BZ1060CCZZ	Screw	N	C	A	A
15	QJAKC1003CCZZ	Jack sockdet		C	A	D
16	PZETL1427CCZZ	Insulator	N	C	A	A
17	LANGT1439CCZZ	Angle B	N	C	A	C
18	QPWBM2027CCZZ	FPC	N	C	A	L
19	LANGT1438CCZZ	Angle A	N	C	A	D
20	XNESD20—16000	Nut		C	A	A
21	QCNCW1293CCZZ	Connector 60pin	N	C	A	Y
22	XBBSD20P06000	Screw		C	A	A
23	LFiX—1116CCZZ	Fixing cushion	N	C	A	B
24	XUBSD20P05000	Screw		C	A	A
25	LANGK1221CCZZ	Fixing angle		C	A	D
26	DUNTK6382CCZZ	Calculation PWB	N	E	B	X
27	CCABA2595CC01	Bottom cabinet (with battery terminal)	N	D	A	N
28	RALMB1006CCZZ	Buzzer		B	A	H
29	QCNCW1294CCZZ	Connector 40pin	N	C	A	X
30	PSLDC1321CCZZ	Seald plate	N	C	A	F
31	XBBSD20P08000	Screw		C	A	A
32	XUBSD20P05000	Screw		C	A	A
33	GWAKP1041CCZZ	Connector angle	N	C	A	F
34	LX—BZ1115CCZZ	Screw	N	C	A	A
35	GFTAU1268CCZZ	Lid for module	N	D	A	C
36	LX—BZ1124CCZZ	Screw	N	C	A	B
37	GFTAB1266CCZZ	Lid for battery	N	D	A	C
38	PSPAP1207CCZZ	Connector spacer	N	C	A	A
39	LX—BZ1114CCZZ	Screw	N	C	A	A
40	LFiX—1126CCZZ	Fixing plate	N	C	A	A
41	LX—NZ1012CCZZ	Nut		C	A	A
42	LX—BZ1113CCZZ	Screw	N	C	A	A
43	PSLDP1334CCZZ	Mask	N	C	A	A
44	LX—BZ1116CCZZ	Screw		C	A	A

NO.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK	
	RC–CZI021CCNI	Capacitor 0.1μF	N	C	A	B
	RC–CZI023CCNI	Capacitor 100PF		C	A	B
	RC–CZI041CCNI	Capacitor 15PF	N	C	A	B
	RC–CZI042CCNI	Capacitor 30PF	N	C	A	B
	RC–EZ105ACCIH	Capacitor 50V/1μF		C	A	B
	RC–EZ227ACCIA	Capacitor 10V/220μF		C	A	C
	RCRSPI036CCZZ	Crystal 32.768KHz		B	A	H
	RCRSZI038CCZZ	Crystal 2.6MHz	N	B	A	E
	RH–DZI005CCNI	Diode DAP202	N	B	A	C
	RH–DZI008CCNI	Diode DAN202	N	B	A	C
	RVR–MB5IOQCZZ	Valiable resistor 250Kohm		C	A	E
	RVR–MI3SB50QC	Valiable resistor 220Kohm	N	C	A	D
	SPAKA6760CCZZ	Packing cushion	N	D	A	D
	SPAKA6881CCZZ	Packing cushion	N	D	A	H
	SPAKC6642CCZZ	Packing case (U.S.A)	N	D	A	K
	SPAKC6761CCZZ	Packing case	N	D	A	F
	TCAUHII8ICCZZ	Caution label for modul		D	A	A
	TiNSE3434CCZZ	Instruction book (U.S.A)	N	D	A	X
	TiNSE3483CCZZ	Instruction book (Others English)	N	D	A	X
	TiNSG35I7CCZZ	Instruction book (Germany)	N	D		
	TiNSM348ICCZZ	Instruction book (E, F, G, S)	N	D		
	TMANEI022CCZZ	Program library (English)	N	D	A	Z
	TMANGI023CCZZ	Program library (Germany)	N	D		
	UBAGCI290CCZZ	Soft case	N	D	A	R
	VHDDSI588LI–I	Diode 1S1588LI		B	A	D
	VHDISS98///–I	Diode	N	B	A	D
	VHHI54KD–5/–I	Thermistor 150Kohm		B	A	C
	VHiEHM7I8L70N	I. C. (Power regurator)	N	B	A	T
	VHiHM6II6//–C	I. C. (HM6116)	N	B	B	H
	VHiLH580I//–I	L. S. I. (LH5801)	N	B	B	K
	VHiLH58II//–I	L. S. I. (LH5811 or 5810)	N	B	A	Z
	VHiSC6I3128FN	L. S. I. (SC613128)	N	B	B	H
	VHiSC882G//–I	L. S. I. (SC882G)		B	A	W
	VHiTC40H000FN	I. C. (TC40H000)	N	B	A	G
	VHiTC40HI38FN	I. C. (TC40H138)	N	B	A	Q
	VHiTC40HI39FN	I. C. (TC40H139)	N	B	A	Q
	VHiTC50H00IFN	I. C. (TC50H001)	N	B	A	H
	VHiTC55I4P/–C	I. C. (TC5514P)	N	B	A	U
	VHiUPDI990ACC	I. C. (μPD1990A)		B	A	T
	VRS–TP2BDI00J	Resistor 1/8W 100ohm		C	A	A
	VRS–TP2BDI02J	Resistor 1/8W 1Kohm		C	A	A
	VRS–TP2BDI03J	Resistor 1/8W 10Kohm		C	A	A
	VRS–TP2BDI04J	Resistor 1/8W 100Kohm		C	A	A
	VRS–TP2BD333J	Resistor 1/8W 33Kohm		C	A	A
	VRS–TP2BD473J	Resistor 1/8W 47Kohm		C	A	A
	VRS–TP2BD562J	Resistor 1/8W 5.6Kohm		C	A	A
	VRS–TP2BD563J	Resistor 1/8W 56Kohm		C	A	A
	VRS–TP2BD564J	Resistor 1/8W 560Kohm		C	A	A
	VS2SC24I2–/–I	Transistor 2SC2412		C	A	C
	LPLTPI090CCZZ	Tenplate	N	D	A	D
			NEW MARK	PARTS RANK	PRICE RANK	

PC–1500–[2]

11 –