SHARP

SERVICE MANUAL

CE-158

SHARP CORPORATION

SERVICE MANUAL
MODEL CE-158
RS-232C Interface
(PC-1500 Option)

CONTENTS

File this manual into the service manual "PC-1500 & Option"

1. INTRODUCTION

There are two types of interfaces built-in. One is a general-purpose interface for the communication between PC-1500 and a device equipped with RS-232C type interface, such as personal computor, peripheral device, etc. The other is a centronics type parallel interface for full-scale data processing printers.

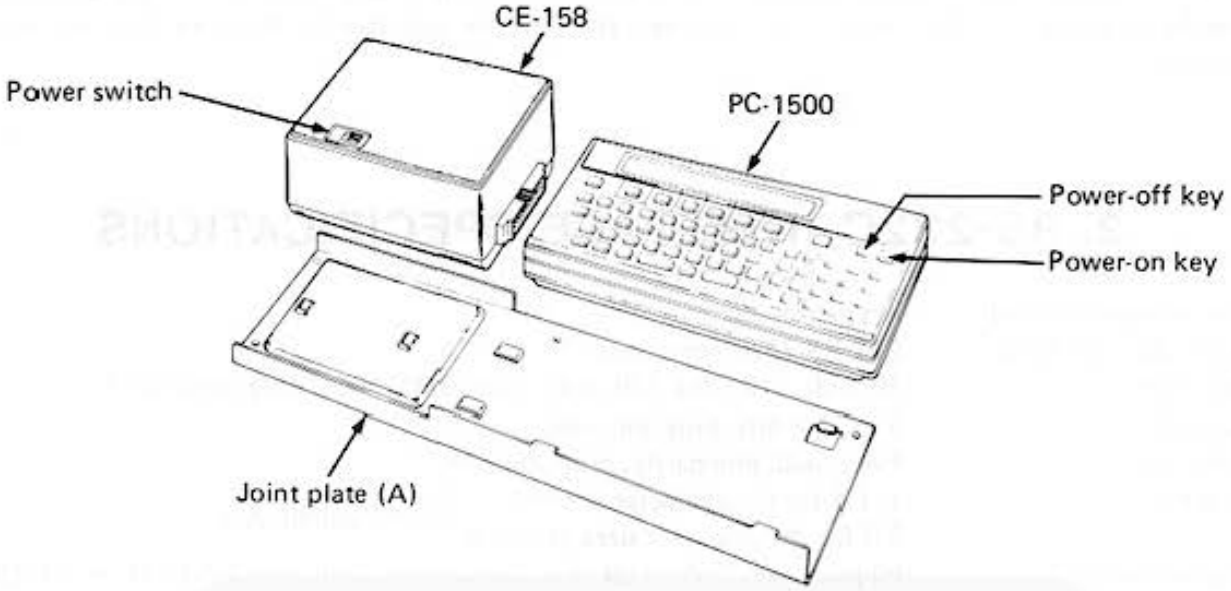
2. RS-232C INTERFACE SPECIFICATIONS

Transmission method	:	Asynchronous
Applicable standards	:	EIA RS-232C compliance
Baud rate	:	50, 100, 110, 200, 300, 600, 1200, 2400 baud, programmable *
Data bit	:	5, 6, 7, 8 bits, programmable
Parity bit	:	Even, odd, non-parity, programmable
Stop bit	:	1, 1.5 for the character size of 5. } programmable 2.0 for the character sizes of 6 to 8. } programmable
Connectors used	:	60-pin male connector for connection with the PC-1500 or CE-150. 25-pin connector, DB-25(W), for connection with an external device. Adaptor jack.
Power supply source	:	4.8 V ⎓ (DC): Ni-Cd rechargeable battery AC: 120 V, 60 Hz with EA-21A
Power consumption	:	4.8 V ⎓ (DC), 0.80 W
AC adaptor/charger	:	EA-21A (120 V, 60 Hz)
Battery capacity	:	For approx. 3 hours of operation (charging: 15 hours)
Output signal level	:	High level: +5 V to +10 V (3 to 7 Kohms load) Low level: −5 V to −10 V (3 to 7 Kohms load)
Interfacing signals	:	Inputs: RD, DSR, CD, CTS Outputs: TD, RTS, DTR Others: SG (FG)
Switch	:	×1 (POWER switch)
Dimensions	:	86 (W) × 115 (D) × 50 (H) mm 3-3/8″ (W) × 4-17/32″ (D) × 1-31/32″ (H)
Weight	:	435 g (0.96 lbs.)
Accessories	:	Keyboard templates, joint plates (two kinds) and instruction manual.

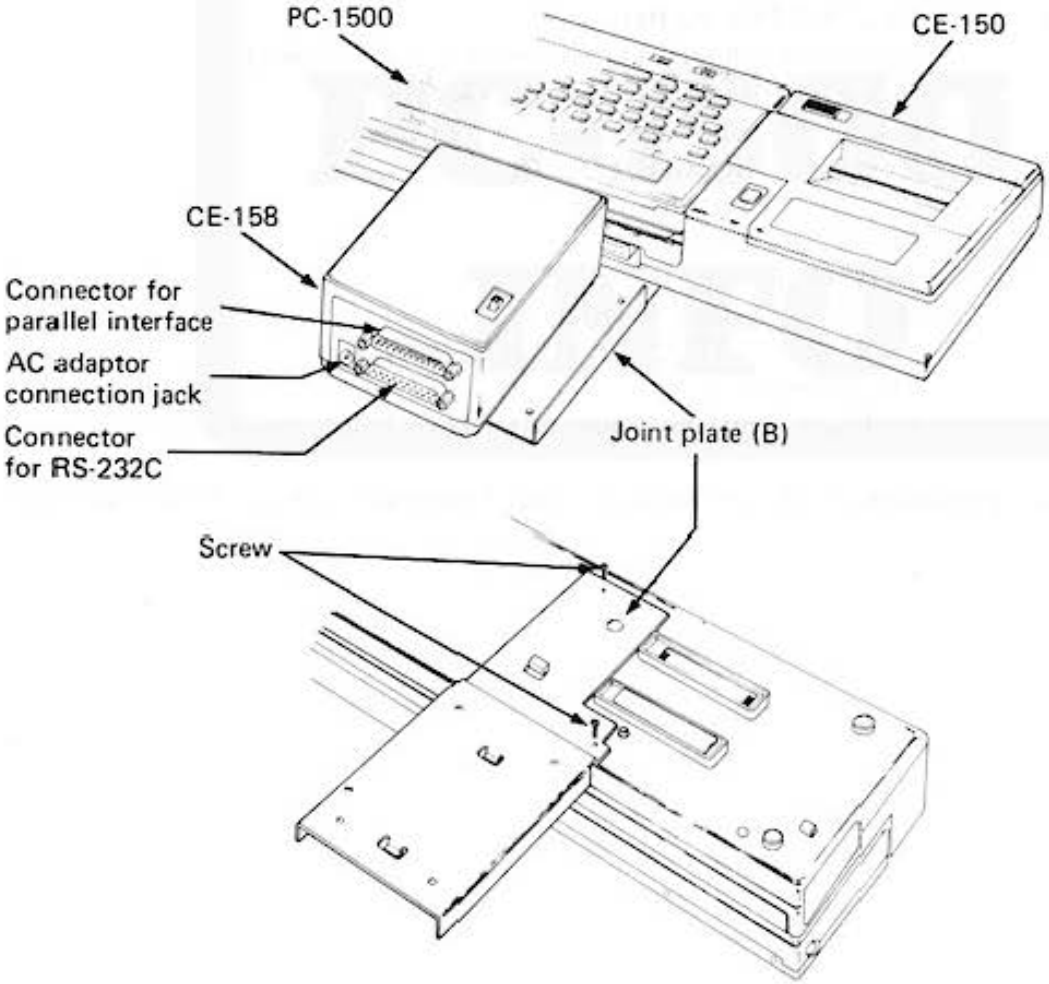
* : In terminal program mode, the specifications of baud rate (600, 1200 and 2400) is restricted.

3. SYSTEM CONFIGURATION

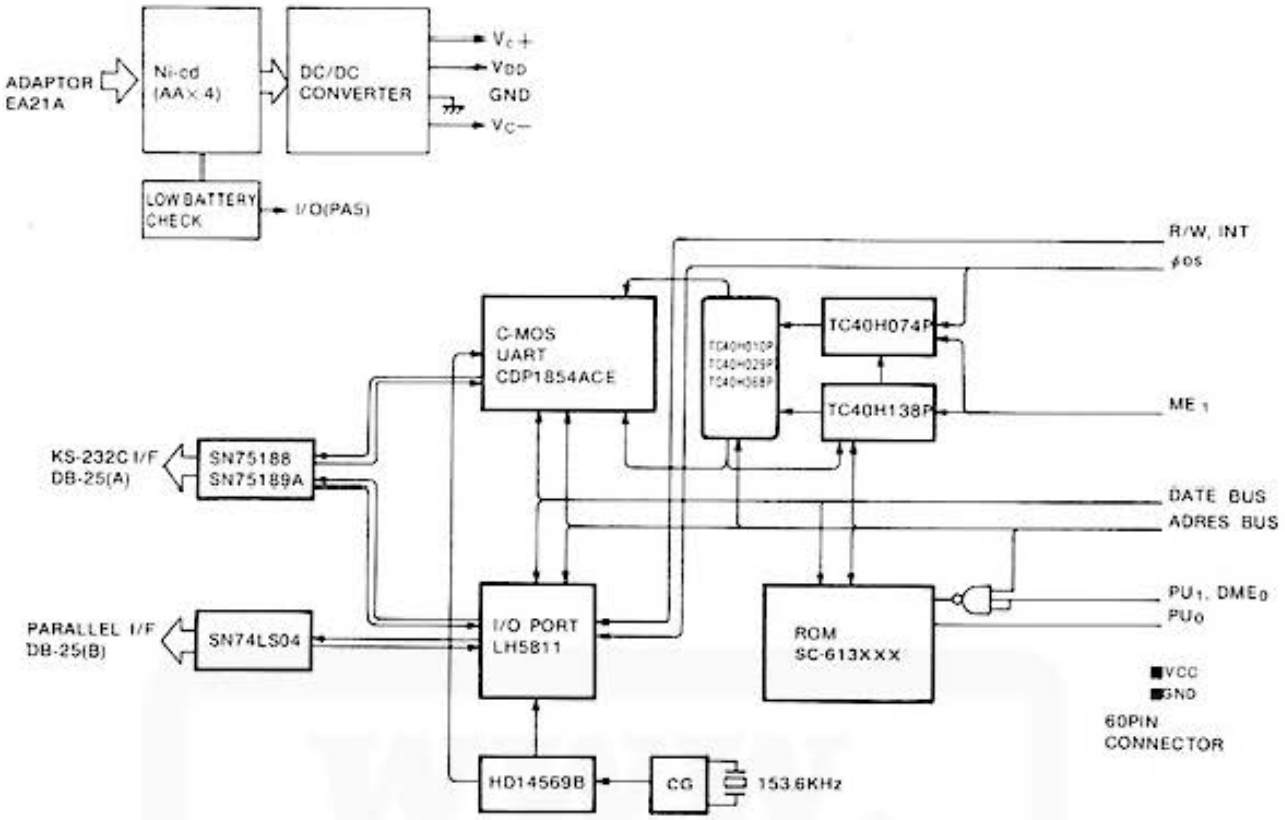
CONNECTION OF PC-1500 WITH CE-158



CONNECTION OF PC-1500 WITH CE-150 AND CE-158



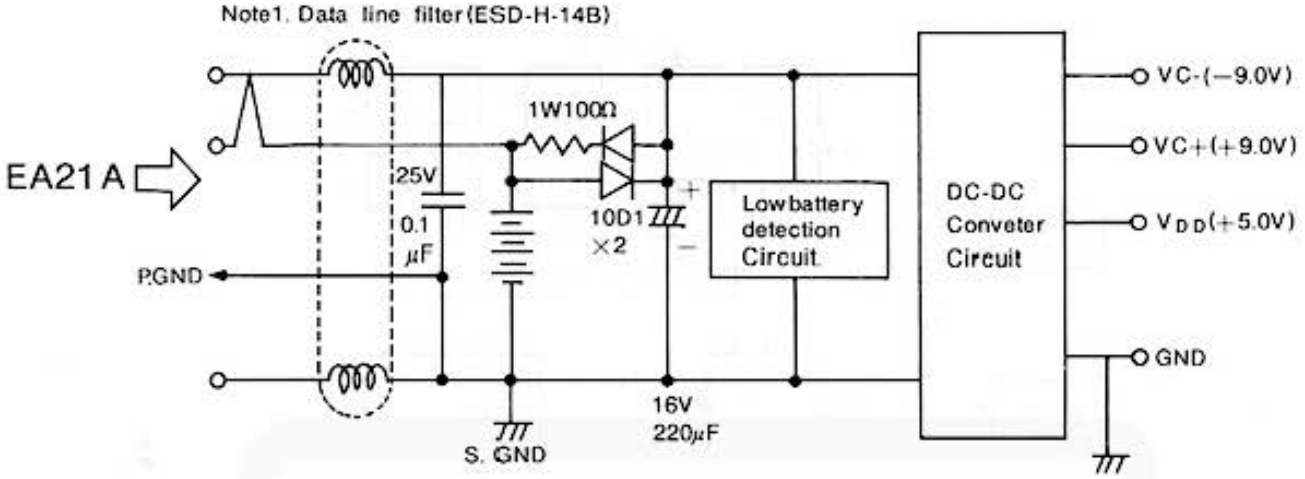
4. BLOCK DIAGRAM



5. CIRCUIT DISCRIPTION

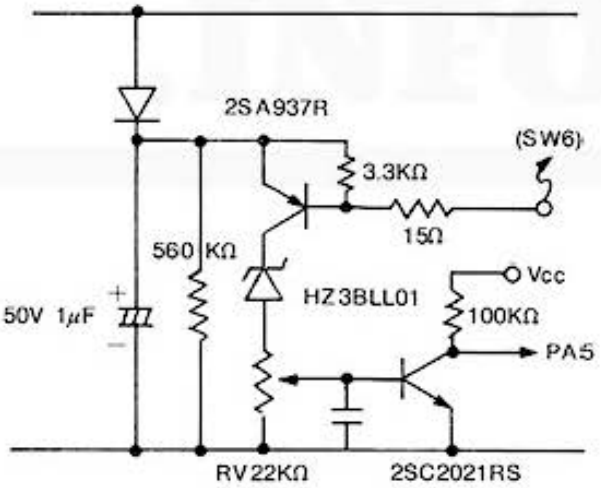
- **Power supply**

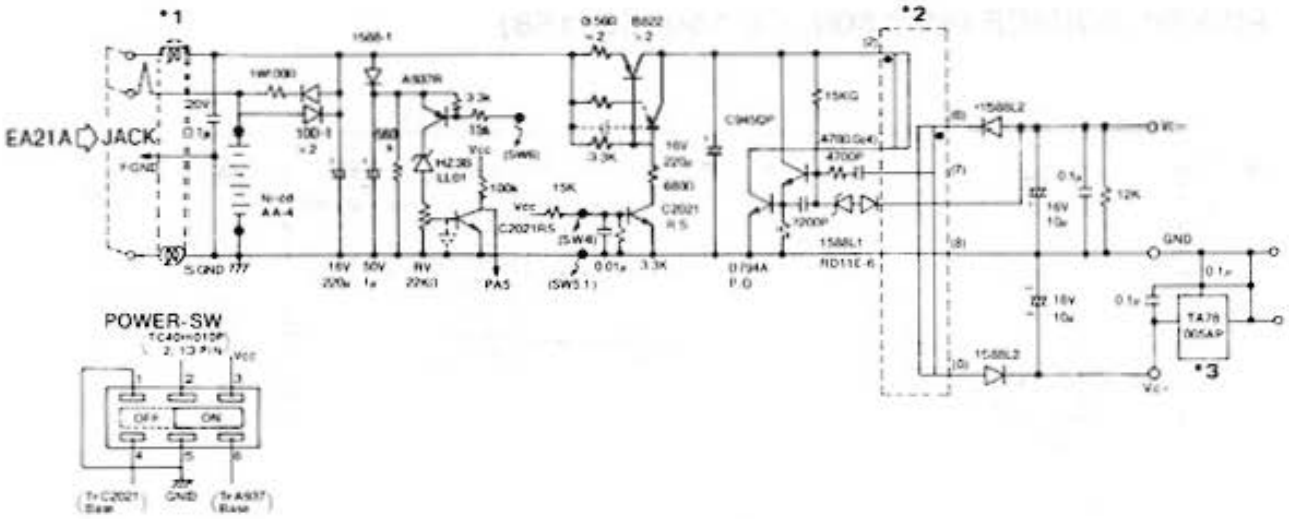
The CE-158 is driven by the PC-1500 power (Vcc) and Ni-Cd battery, or through an AC adapter. The input is fed through the DC-DC converter to reach VDD (+5.0 V), VC+ (+9.0 V), and VC– (–9.0 V).



- **Low battery detection circuit**

Battery condition is monitored by the circuit sketched below. Signals detected are checked by the CPU for each receiving and transmitting step through LH5811's PA5 I/O port. Besides, SW6 reaches the GND level with power on, thereby turning on 2SA937R to keep the low battery detection circuit in function.

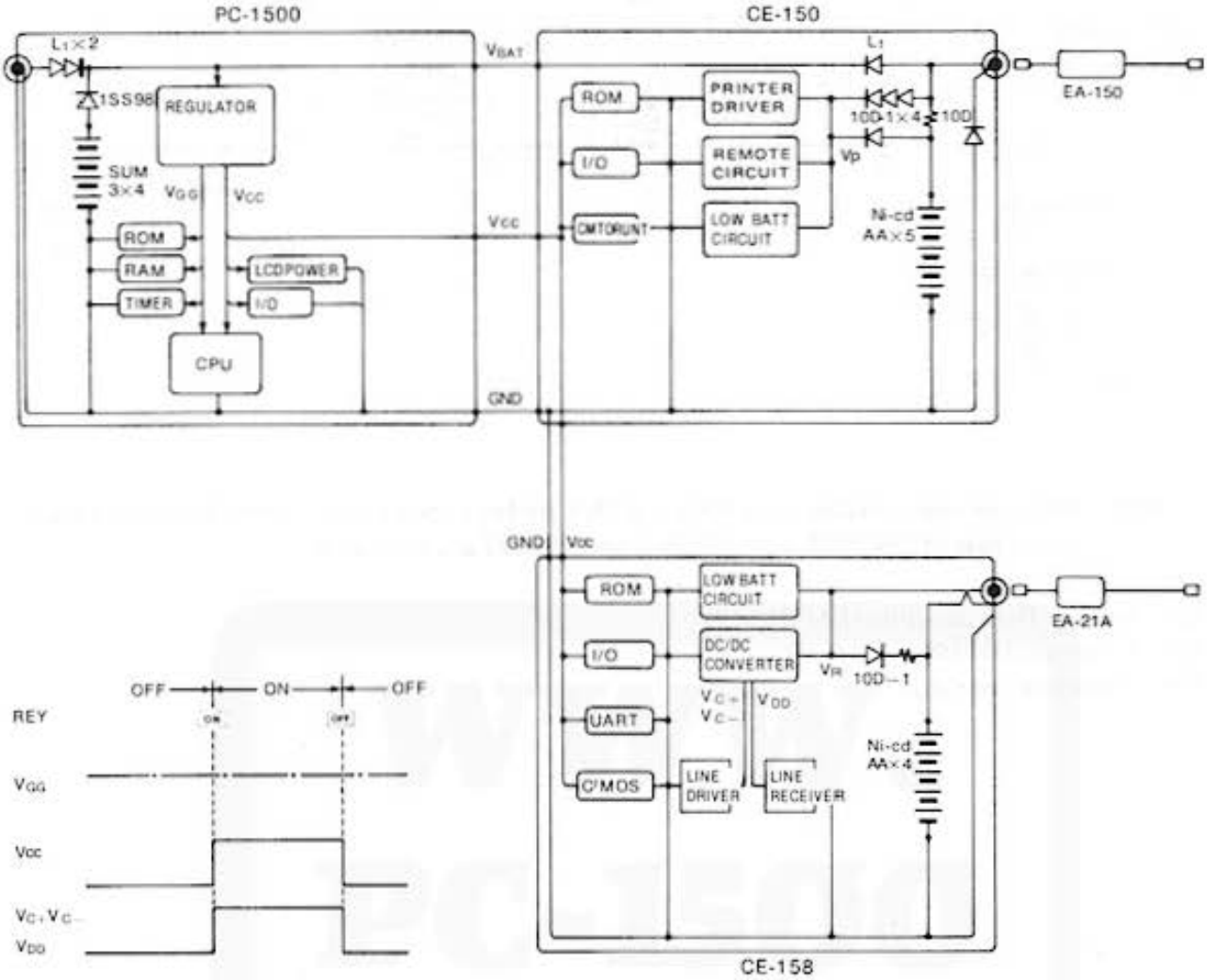


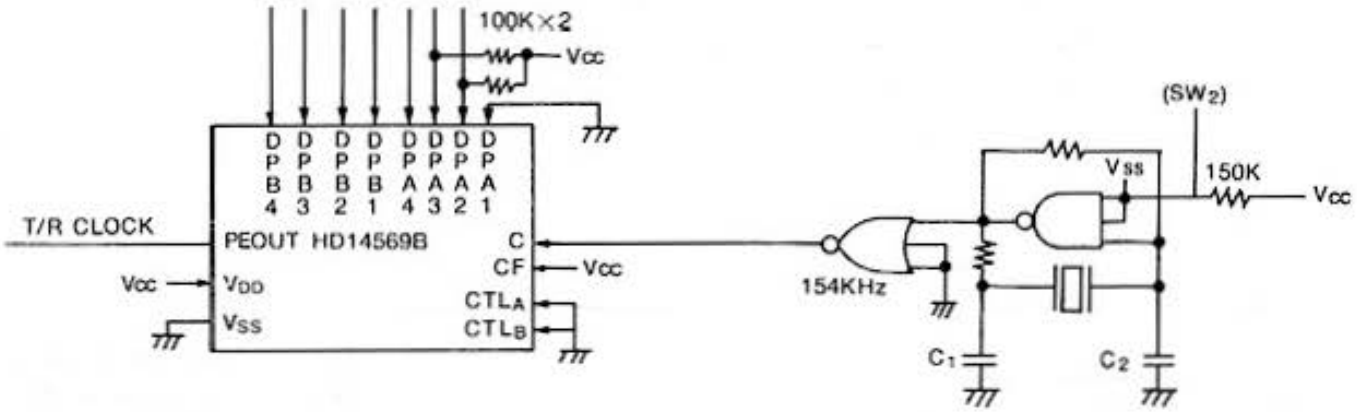


Note: While the power switch is on, SW4 and SW5 are kept open to each other. Vcc is impressed to the base of 2SC2021, and 2SC2021 and 2SB822 are turned on.

*1) Note 1: Data line filter (ESD-H-14B)
*2) Converter H1750
*3) 3-terminal regulator

POWER SOURCE (PC-1500, CE-150, CE-158)





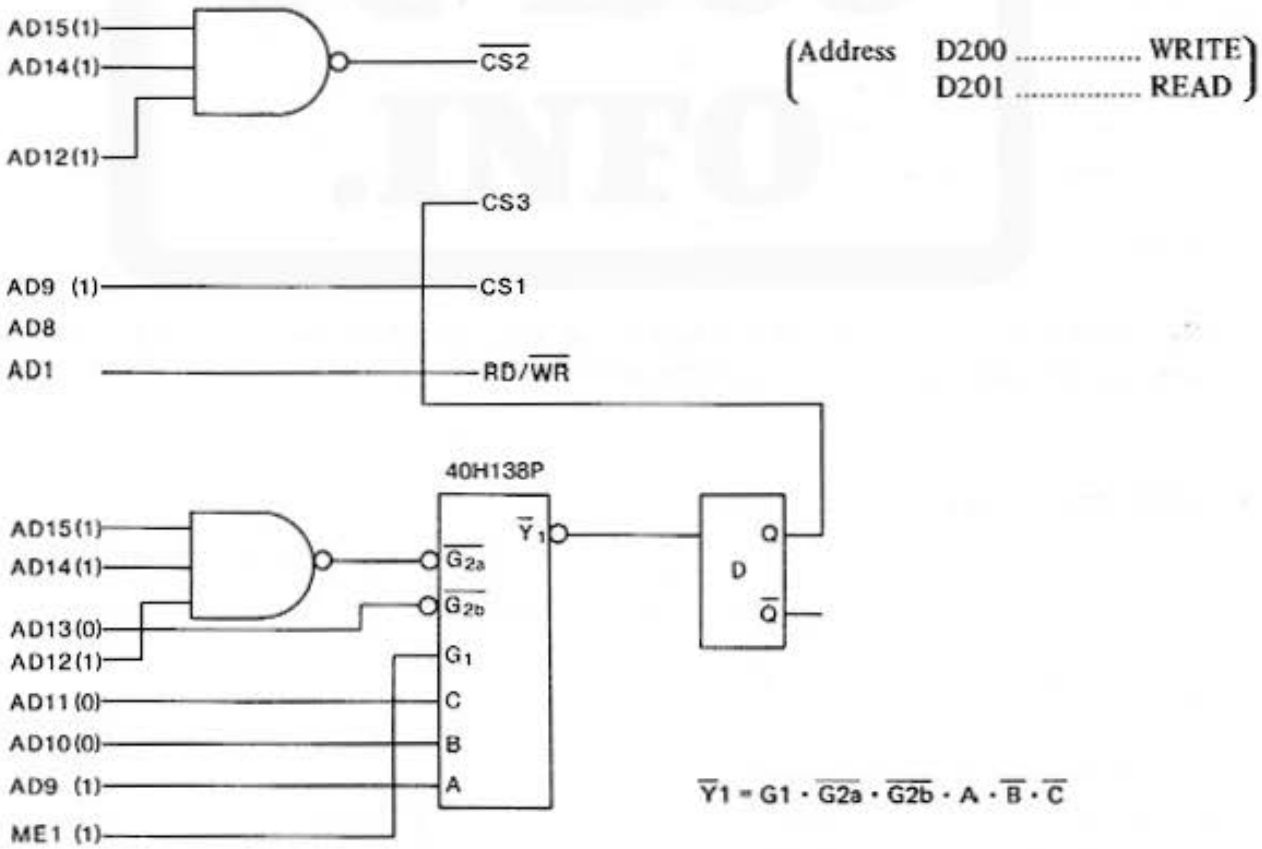
- **CLOCK circuit**

  According to commands from the CPU, the frequency dividing ratio is changed to make a clock pulse corresponding to respective baud rates. In initial setting, after turning the power switch on, the baud rate of 300 is automatically provided. Thus a specified baud rate can be obtained with change command from the CPU. The commands are delivered to LH5811 ports PC0 thru PC4, PA6 or PA7. (T/R clock = baud rate X 16)

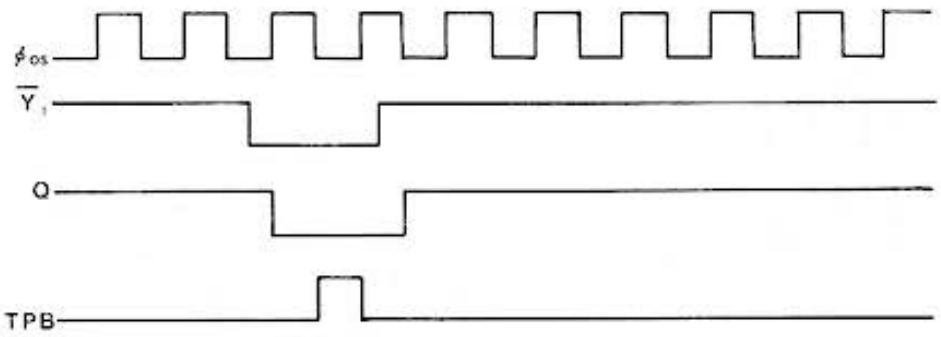
- **CDP1854ACE CHIP SELECT**

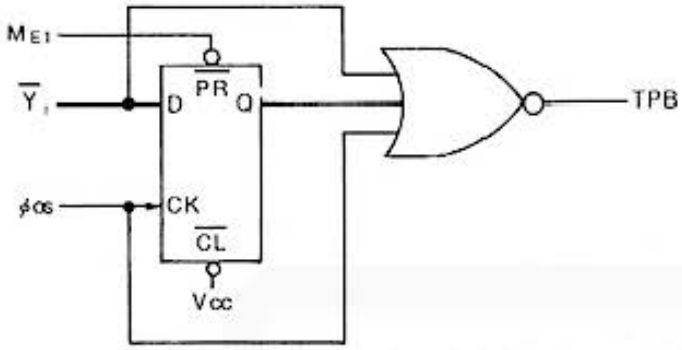
  The conditions to select this chip are that CS1 and CS3 are at HIGH position and that $\overline{CS2}$ is at LOW position.

  The circuit is as shown below.



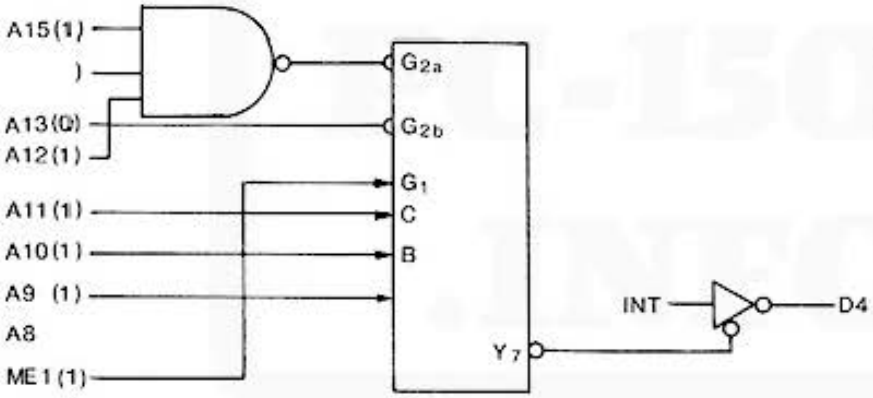
- **TPB CIRCUIT**





The left-hand circuit is to produce one pulse at ME_1 ($\overline{Y}_1$). At Y_1 and ϕ_{OS}, however, two pulses are generated up to TPB. Therefore, a stage of DFF is added to produce signal Q. Thus TPB consists of Y_1, Q, and ϕ_{OS}.

- **INT CIRCUIT**

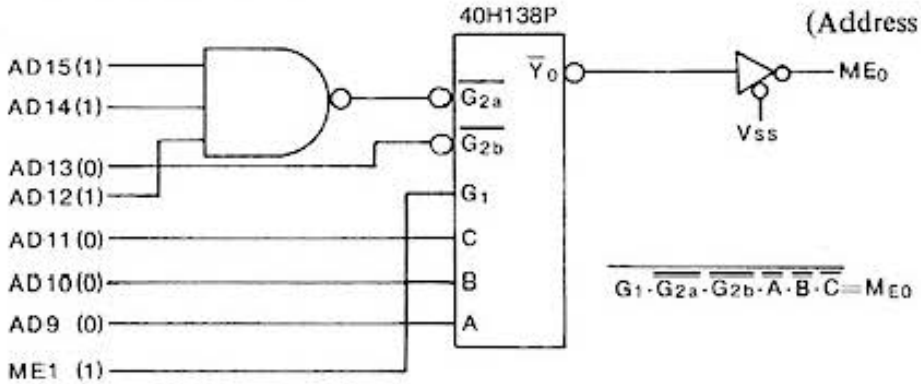


INTERRUPT PORT ADDRESS

$ME_1\left(\begin{matrix}DE00\\ \wr \\ DFFF\end{matrix}\right)$

INTERRUPT will be effective only condition of ME1, A9, A10, A11, A12, AB A14, A15, (Interrupt will proceed adress of between DE00 to DFFF)

- **LH5811 CHIP SELECT**



(Address D000 or D00F to be used)

6. LSI Discription

CDP1854A, CDP1854AC Types

1. Initialization and Controls

In this mode, the CDP1854A is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the RD/$\overline{WR}$ and RSEL inputs as follows:

TABLE 1-Register Selection Summary

RSEL	RD/$\overline{WR}$	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Hodling Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	Low	Read Status Register from Receiver Bus

In this mode the CDP1854A is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. The CLEAR input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1 · CS2 · CS3-1) and the Control Register is designated (RSEL = H. RD/$\overline{WR}$ = L). The CDP1854A also has a Status Register which can be read onto the Receiver Bus (R BUS 0-R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Fig. 7.

2. Transmitter Operation

Before beginning to transmit, the TBANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, Fig. 3) is set. Loading the Control Register with TR = 1 (bit 7 = high) inhibits changing the other control bits. Therefore two loads are required: one to format the UART, the second to set TR. When TR has been set, a TRANSMITTER HOLDING REGISTER EMPTY ($\overline{THRE}$) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the REQUEST TO SENT (RTS) output to the peripheral. It is not necessary to set TR for proper operation for the UART. If desired, it can be used to enable $\overline{THRE}$ interrupts and to generate the $\overline{RTS}$ signal. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854A is selected by CS1 · CS2 · CS3 = 1, and the Holding Register is selected by RSEL = L and RD/$\overline{WR}$ = L. When the CLEAR $\overline{TO\ SEND}$ ($\overline{CTS}$) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If CTS is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least 1/2 clock period after the trailing edge of TPB and transmission of a start bit will occur 1/2 clock period later (see Fig. 1). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the transmitter shift register will not be transmitted.

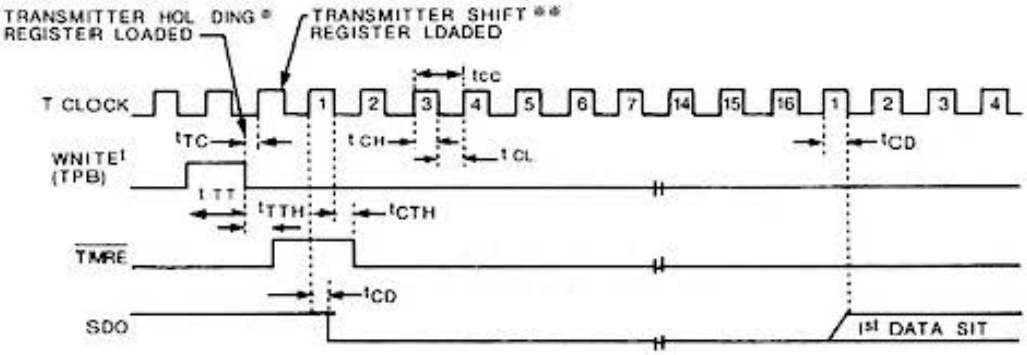
One transmitter clock period after the Transmitter Shfit Register is loaded from the Transmitter Holding Register, the $\overline{THRE}$ signal will go low and an interrupt will occur ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE · TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by

reloading the original control byte in the Control Register with the TR bit = 0, thus terminating the REQUEST TO SEND ($\overline{RTS}$) signal.
SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Fig. 6). SDO is held low until the BREAK bit is reset.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, t_r, t_f −20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Figs. 1 and 2.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP-1854AC		
			Typ.•	Max.▲	Typ.•	Max.▲	
Trransmitter Timing – MODE 1							
Minimum Clock Period	t_{CC}	5 10	250 125	310 155	250 –	310 –	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	100 75	125 100	100 –	125 –	ns
Clock High Level	t_{CH}	5 10	100 75	125 100	100 –	125 –	ns
TPB	t_{TT}	5 10	100 50	150 75	100 –	150 –	ns
Minimum Setup Time: TPB to Clock	t_{TC}	5 10	175 90	225 150	175 –	225 –	ns
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5 10	300 150	450 225	300 –	450 –	ns
TPB to $\overline{THRE}$	t_{TTH}	5 10	200 100	300 150	200 –	300 –	ns
Clock to $\overline{THRE}$	t_{CTH}	5 10	200 100	300 150	200 –	300 –	ns
CPU Interface – WRITE Timing – MODE 1							
Minimum Pulse Width: TPB	t_{TT}	5 10	100 50	150 75	100 –	150 –	ns
Minimum Setup Time: RSEL to Write	t_{RSW}	5 10	50 25	74 40	50 –	75 –	ns
Data to Write	t_{DW}	5 10	−100 −50	− 75 −35	100 –	−75 –	ns
Minimum Hold Time: RSEL after Write	t_{WRS}	5 10	50 25	75 40	50 –	75 –	ns
Data after Write	t_{WD}	5 10	75 40	125 60	75 –	125 –	ns

• Typical values are for T_A = 25°C and nominal voltages.
▲ Maximum limits of minimum characteristics are the values above which all devices function.

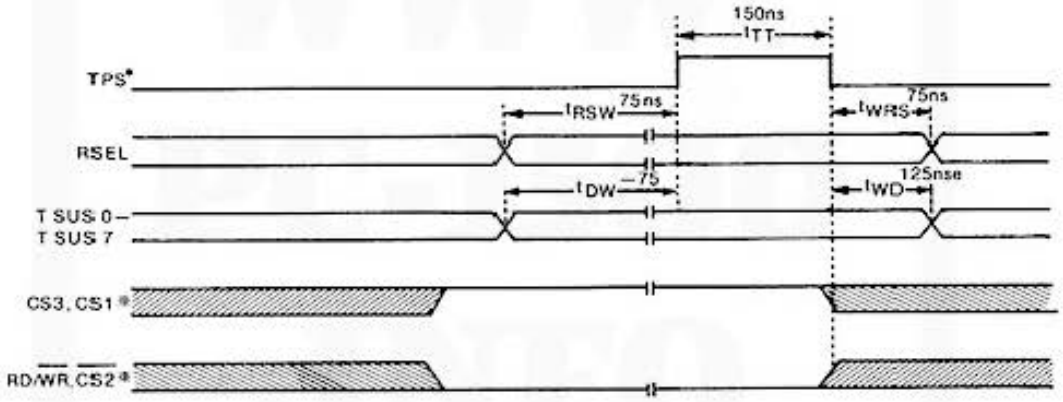


* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF TPB

** THE TRANSMITTER SHIFT REGISTER IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{TC} AFTER THE TRAILING EDGE OF TPB, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER.

† WRITE IS THE OVERLAP OF TPB, CS1, AND CS3 = I AND $\overline{CS3}$, RD/$\overline{WR}$ · O.

Fig. 1 – Transmitter timing diagram – MODE 1.



* WRITE IS THE OVERLAP OF TPB, CSI, CS3 = I AND $\overline{CS2}$, RD/$\overline{WR}$ · O.

Fig. 2 – MODE 1 cpu interface (WRITE) timing diagram.

CONTROL REGISTER BIT ASSIGNMENT TABLE

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Bit Signal: Function

0 PARITY INHIBIT (PI):
When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bits(s) will immediately follow the last data bit on transmission, and EPE is ignored.

1 EVEN PARITY ENABLE (EPE):
When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.

2 STOP BIT SELECT (SBS):
See table below.

3 WORD LENGTH SELECT 1 (WLS1):
See table below.

4 WORD LENGTH SELECT 2 (WLS2):
See table below.

Bit 4 WLS2	Bit 3 WLS1	Bit 2 SBS	Function
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

Fig. 3 – Control Registar bit assignment.

5 INTERRUPT ENABLE (IE):
When set high $\overline{\text{THRE}}$, DA, THRE · TSRE, $\overline{\text{CTS}}$, and PSI interrupts are enabled (see Interrupt Conditions, Table II).

6 TRANSMIT BREAK (BREAK):
Holds SDO low when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low and one of the following occurs: $\overline{\text{CLEAR}}$ goes low; $\overline{\text{CTS}}$ goes high; or a word is transmitted. (The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of all zeros).

7 TRANSMIT REQUEST (TR):
When set high, $\overline{\text{RTS}}$ is set low and data transfer through the transmitter is initiated by the initial $\overline{\text{THRE}}$ interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops.)

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-lavel input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 7-1/2 in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused most significant bits. If $\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the Data Available status bit is also set and the $\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$) and $\overline{\text{INTERRUPT}}$ ($\overline{\text{INT}}$) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's 3-state bus drivers are enabled when the UART is selected ($\overline{\text{CS1}} \cdot \text{CS2} \cdot \text{CS3} = 1$) and RD/WR = high. Status can be read when RSEL = high. Data is read when RSEL = Low. When reading data, TPB latches data in the microprocessor and resets $\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

STATUS REGISTER BIT ASSIGNMENT TABLE

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	–	–	–	14	15	15	19*

* Polarity reversed at output terminal.

Fig. 4 – Status Register bit assignment

BIT SIGNAL: FUNCTION

0 DATA AVAILABLE (DA):
When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19 but with its polarity reversed.

1 OVERRUN ERROR (OE):
When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term. 15.

2 PARITY ERROR (PE):
When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term. 15.

3 FRAMING ERROR (FE):
When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.

4 EXTERNAL STATUS (ES):
This bit is set high by a low-level input at Term. 38 ($\overline{\text{ES}}$).

5 PERIPHERAL STATUS INTERRUPT (PSI):
This bit is set high by a high-to-low voltage transition of Term. 37 ($\overline{PSI}$). The INTERRUPT output (Term. 13) is also asserted ($\overline{INT}$ = low) when this bit is set.

6 TRANSMITTER SHIFT REGISTER EMPTY (TSRE):
When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.

7 TRANSMITTER HOLDING REGISTER EMPTY (THRE):
When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also sets the $\overline{THRE}$ output (Term. 22) low and causes an INTERRUPT ($\overline{INT}$ = low), if TR is high.

4. Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The $\overline{REQUEST\ TO\ SETNT}$ ($\overline{RTS}$) output signal alerts the peripheral to get ready to receive data. The $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input signal is the response, signalling that the peripheral is ready. The $\overline{EXTERNAL\ STATUS}$ ($\overline{ES}$) input latches a peripheral status level, and the $\overline{PERIPHERAL\ STATUS\ INTERRUPT}$ ($\overline{PSI}$) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modern $\overline{DATA\ CARRIER\ DETECT}$ line could be connected to the $\overline{PSI}$ input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (See Fig. 4).

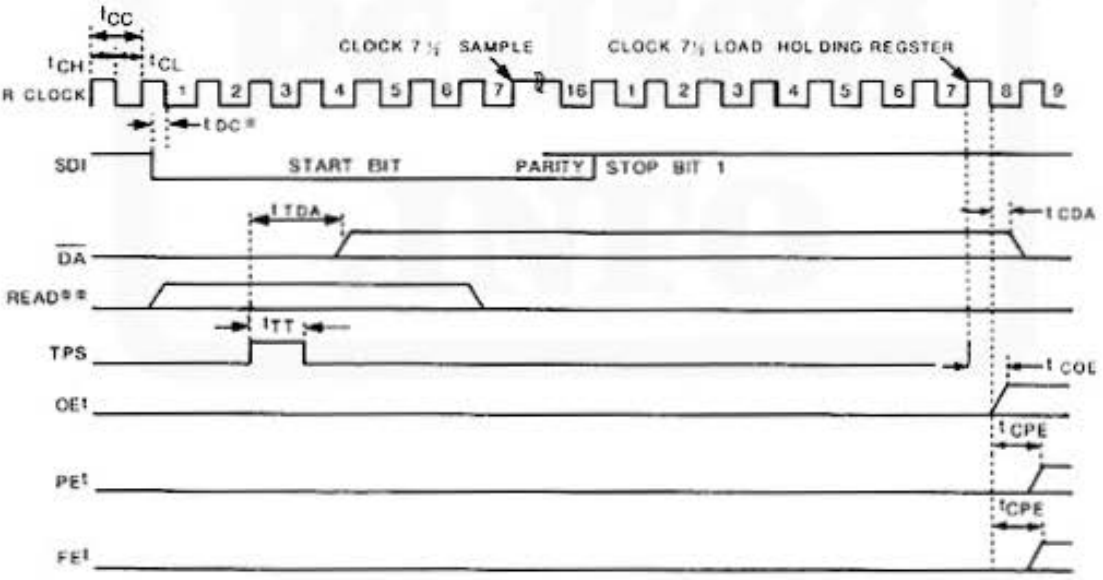


Fig. 5 — MODE 1 receiver timing diagram.

* IF A START BIT OCCURS AT A TIME LESS THAN T_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

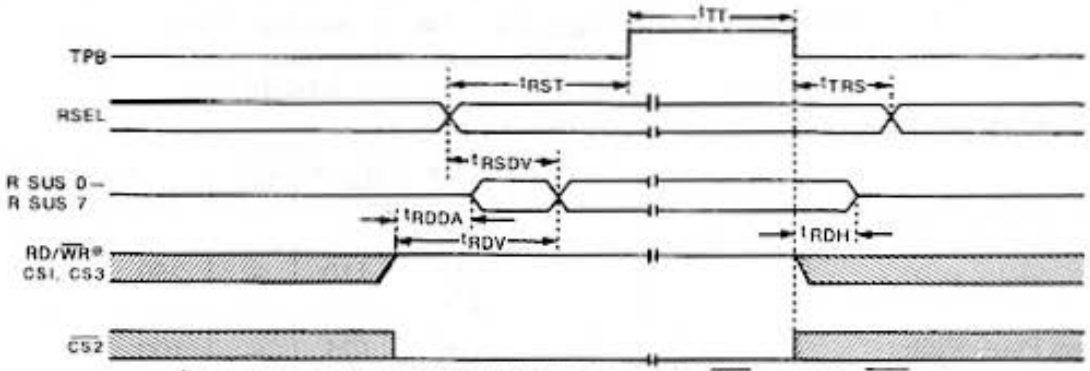
** READ IS THE OVERLAP OF CSI, CS3, RD/$\overline{WR}$ = 1 AND $\overline{CS2}$ = 0.
IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

† OE AND PE SHARE TERMINAL 15 AND ARE ALSO AVAILABLE AS TWO SEPARATE BITS IN THE STATUS REGISTER.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, D_L = 100 pF. See Figs. 5 and 6.

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1854A			CDP1854AC			
			Min.	Typ.•	Max.▲	Min.	Typ.•	Max.▲	
Receiver Timing – MODE 1									
Minimum Clock Period	t_{CC}	5 10	– –	250 125	310 155	– –	250 –	310 –	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	– –	100 75	125 100	– –	100 –	125 –	ns
Clock High Level	t_{CH}	5 10	– –	100 75	125 100	– –	100 –	125 –	ns
TPB	t_{TT}	5 10	– –	100 50	150 75	– –	100 –	150 –	ns
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5 10	– –	100 50	150 75	– –	100 –	150 –	ns
Propagation Delay Time: TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	5 10	– –	220 110	325 175	– –	220 –	325 –	ns
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5 10	– –	220 110	325 175	– –	220 –	325 –	ns
Clock to Overrun Error	t_{COE}	5 10	– –	210 105	300 150	– –	210 –	300 –	ns
Clock to Parity Error	t_{CPE}	5 10	– –	240 120	375 175	– –	240 –	375 –	ns
Clock to Framing Error	t_{CFE}	5 10	– –	200 100	300 150	– –	200 –	300 –	ns
CPU Interface – READ Timing – MODE 1									
Minimum Pulse Width: TPB	t_{TT}	5 10	– –	100 50	150 75	– –	100 –	150 –	ns
Minimum Setup Time: RSEL to TPB	t_{RST}	5 10	– –	50 25	75 40	– –	50 –	75 –	ns
Minimum Hold Time: RSEL after TPB	t_{TRS}	5 10	– –	50 25	75 40	– –	50 –	75 –	ns
Read to Data Access Time	t_{RDDA}	5 10	– –	200 100	300 150	– –	200 –	300 –	ns
Read to Data Valid Time	t_{RDV}	5 10	– –	200 100	300 150	– –	200 –	300 –	ns
RSEL to Data Valid Time	t_{RSDV}	5 10	– –	150 75	225 125	– –	150 –	225 –	ns
Hold Time: Data after Read	t_{RDM}	5 10	50 25	150 75	– –	50 –	150 –	– –	ns

• Typical values are for T_A = 25°C and nominal voltages.
▲ Maximum limits of minimum characteristics are the values above which all devices function.



* READ IS THE OVERLAP OF CS1, CS3, RD/$\overline{WR}$ = 1 AND $\overline{CS2}$ = 0

Fig. 6 – MODE 1 cpu interface (READ) timing diagram

TABLE 2-Interrupt Set and Reset Conditions

SET* ($\overline{INT}$ = LOW)	RESET ($\overline{INT}$ = HIGH)	
CAUSE	CONDITION	TIME
DA (Receipt of data)	Read of data	TPB leading edge
THRE▲ (Ability to reload)	Read of status or write of character	TPB leading edge
THRE · TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
$\overline{PSI}$ (Negative edge)	Read of status	TPB trailing edge
$\overline{CTS}$ (Positive edge when $\overline{THRE \cdot TSRE}$)	Read of status	TPB leading edge

* Interrupts will occur only after the IE bit in the Control Register (see Fig. 3) has been set.

▲ THRE will cause an interrupt only after the TR bit in the Control Register (see Fig. 3) has been set.

FUNCTIONAL DEFINITIONS FOR CDP1854A TERMINALS MODE 1

SIGNAL: FUNCTION

V_{DD}:
Positive supply voltage

MODE SELECT (MODE):
A high-level voltage at this input selects MODE 1 operation.

V_{SS}:
Ground

$\overline{CHIP\ SELECT\ 2}$ ($\overline{CS2}$):
A low-level voltage at this input together with CS1 and CS3 selects the CDP1854A UART.

RECEIVER BUS (R BUS 7 - R BUS 0):
Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).

$\overline{INTERRUPT}$ ($\overline{INT}$):
A low-level voltage at this output indicates the presence of one of more of the interrupt conditions listed in Table 2.

FRAMING ERROR (FE):
A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.

PARITY ERROR or OVERRUN ERROR (PE/OE):
A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Fig. 4).

REGISTER SELECT (RSEL):
This input is used to choose either the Control/Status Register (high input) or the transmitter/receiver data registers (low input) according to the truth table in Table 1.

RECEIVER CLOCK (RCLOCK):

Clock input with a frequency 16 times the desired receiver shift rate.

TPB:

A positive input pulse used as a data load or reset strobe.

$\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$)

A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):

Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

$\overline{\text{CLEAR}}$ ($\overline{\text{CLEAR}}$):

A low-level voltage at this input resets the Interrupt Flip-Flop, Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.

$\overline{\text{TRANSMITTER HOLDING REGISTER EMPTY}}$ ($\overline{\text{THRE}}$):

A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

CHIP SELECT 1 (CS1):

A high-level voltage at this input together with $\overline{\text{CS2}}$ and CS3 selects the UART.

$\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$):

This output signal tells the peripheral to to get ready to receive data. $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) is the response from the peripheral. $\overline{\text{RTS}}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.

SERIAL DATA OUTPUT (SDO):

The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s) are serially shifted out on this output. When no character is being transmitted, at high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):

Transmitter parallel data input. These may be externally connected to corresponding Receiver bus terminals.

RD/$\overline{\text{WR}}$:

A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.

CHIP SELECT 3 (CS3):

With high-level voltage at this input together with CS1 and $\overline{\text{CS2}}$ selects the UART.

$\overline{\text{PERIPHERAL STATUS INTERRUPT}}$ ($\overline{\text{PSI}}$):

A high-to-low transition on this input line sets a bit in the Status Register and causes an $\overline{\text{INTERRUPT}}$ ($\overline{\text{INT}}$ = low).

$\overline{\text{EXTERNAL STATUS}}$ ($\overline{\text{ES}}$):

A low-level voltage at this input sets a bit in the Status Register.

$\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$):

When this input from peripheral is high, transfer of a character to the Transmitter Shifrt Register and shifting of serial data out is inhibited.

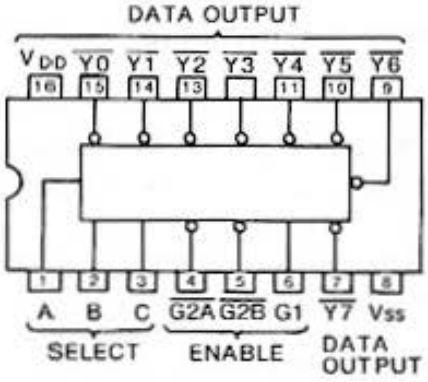
TRANSMITTER CLOCK (TCLOCK):

Clock input with a frequency 16 times the desired transmitter shift rate.

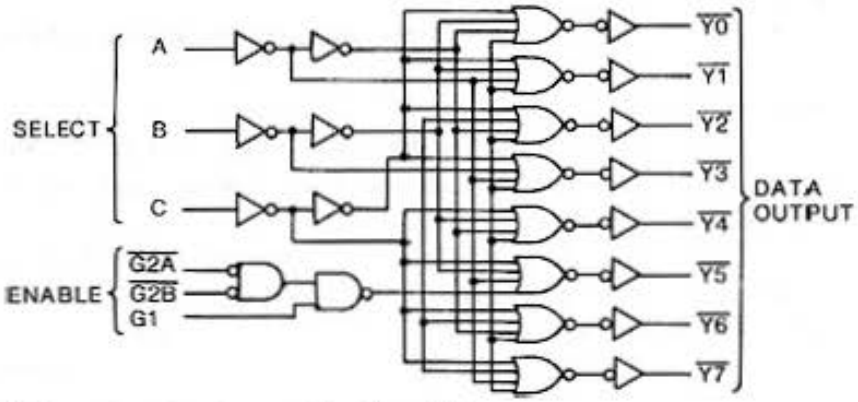
7. IC PIN CONNECTION

TC40H138P

Pin connections



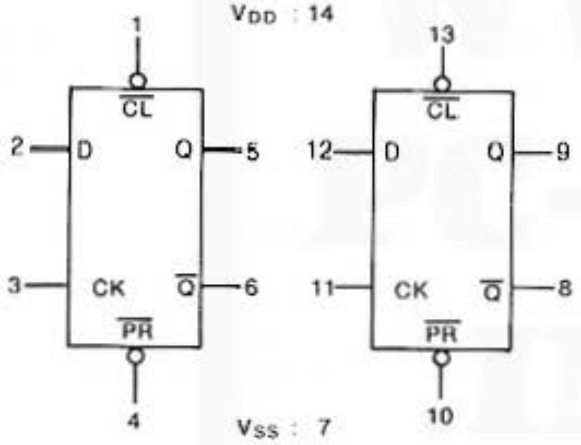
Logic diagram



* Protective circuits provided for all inputs

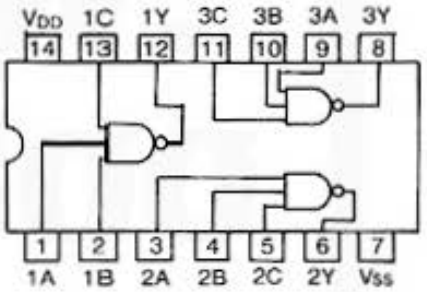
TC40H074P

Block diagram

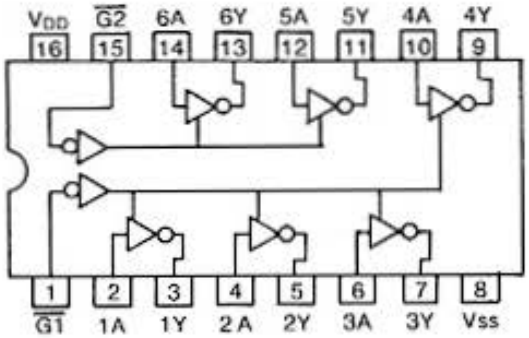


TC40H010P

Pin connections

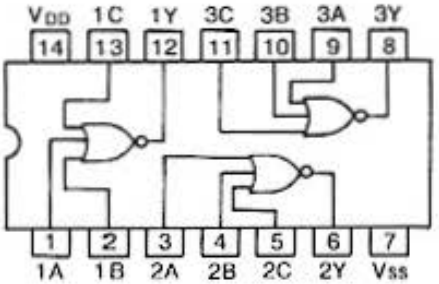


TC40H368P



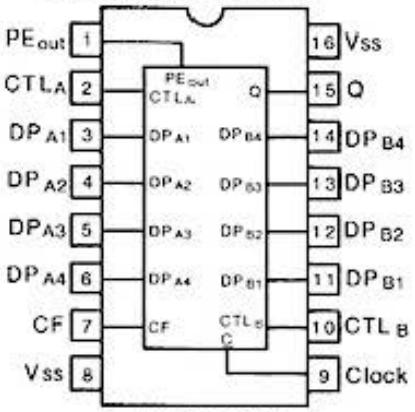
TC40H027P

Pin connections



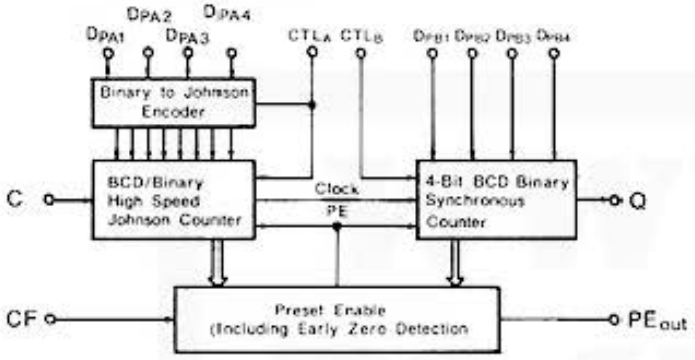
HD14569B

- **PIN ARRANGEMENT**



TOP VIEW

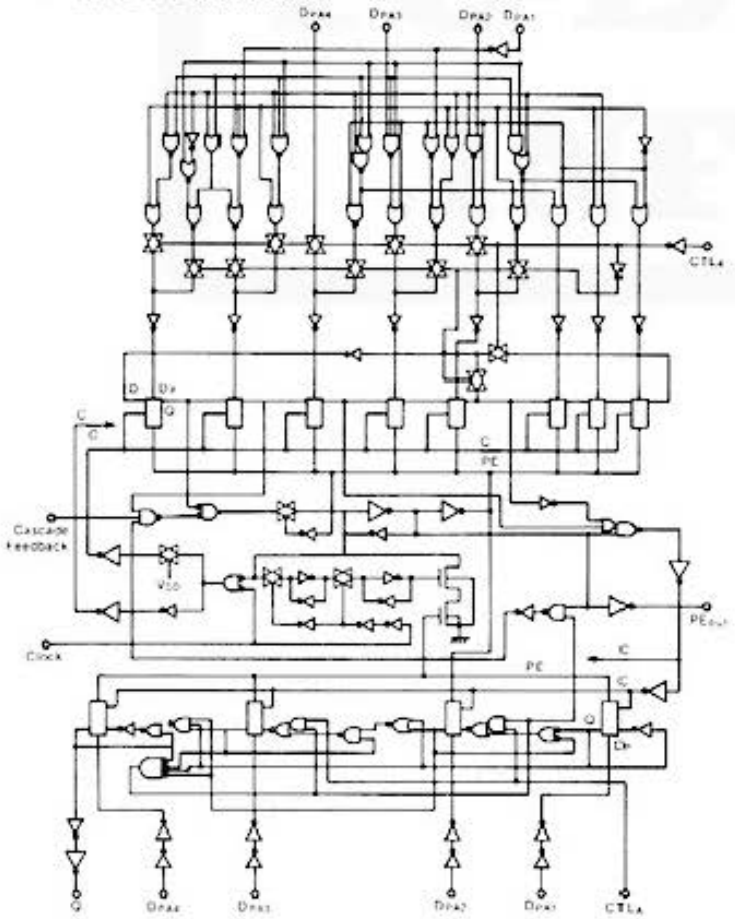
- **BLOCK DIAGRAM**



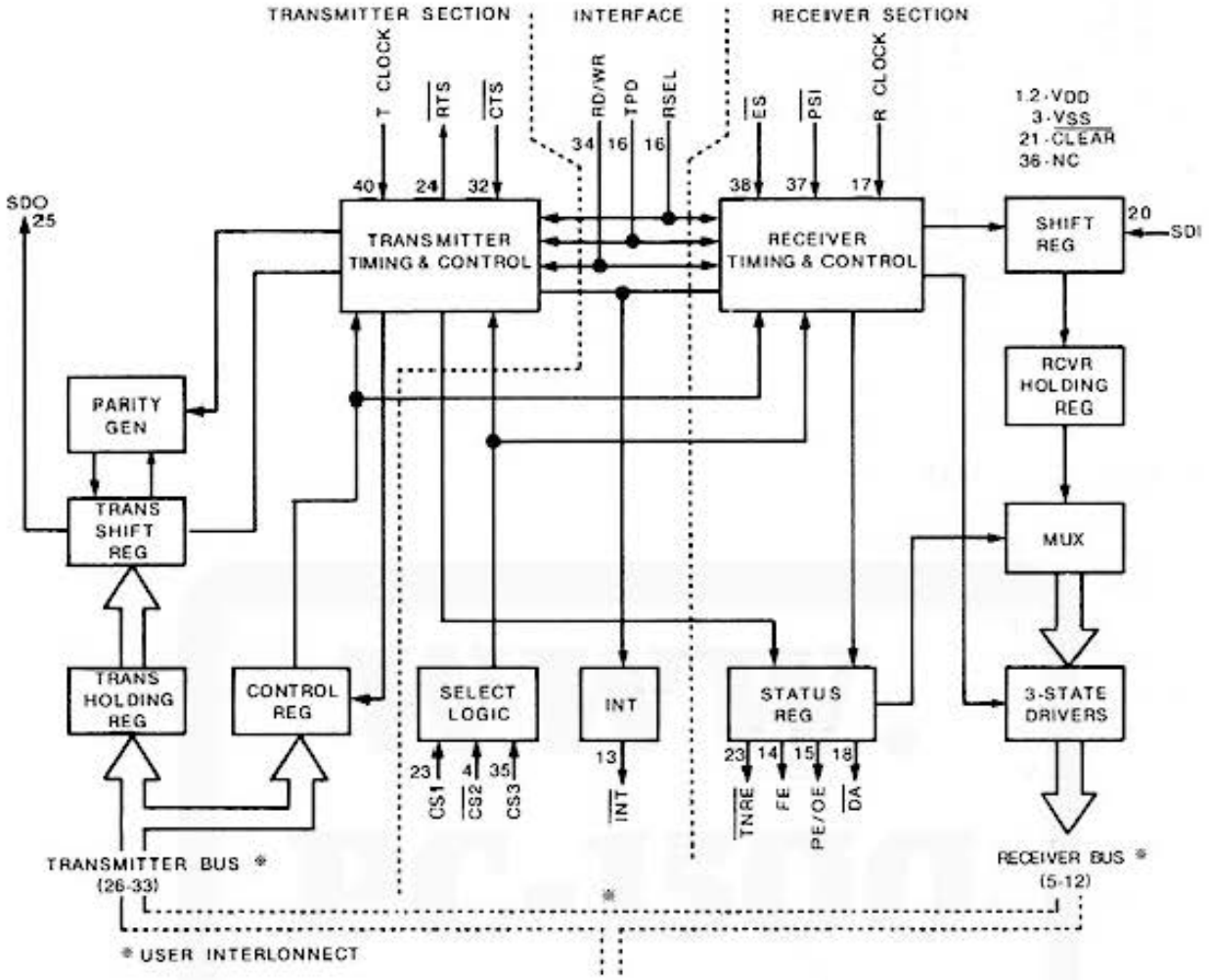
CTL = "O" AT BINARY COUNTING

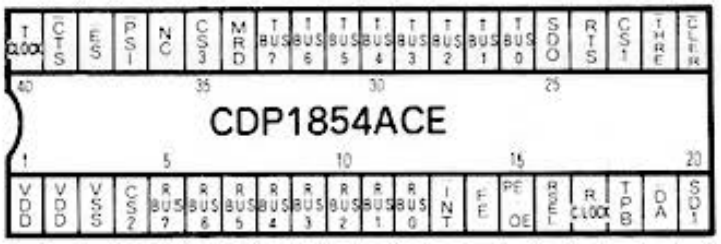
CTL = "1" AT BCD COUNTING

- **LOGIC DIAGRAM**

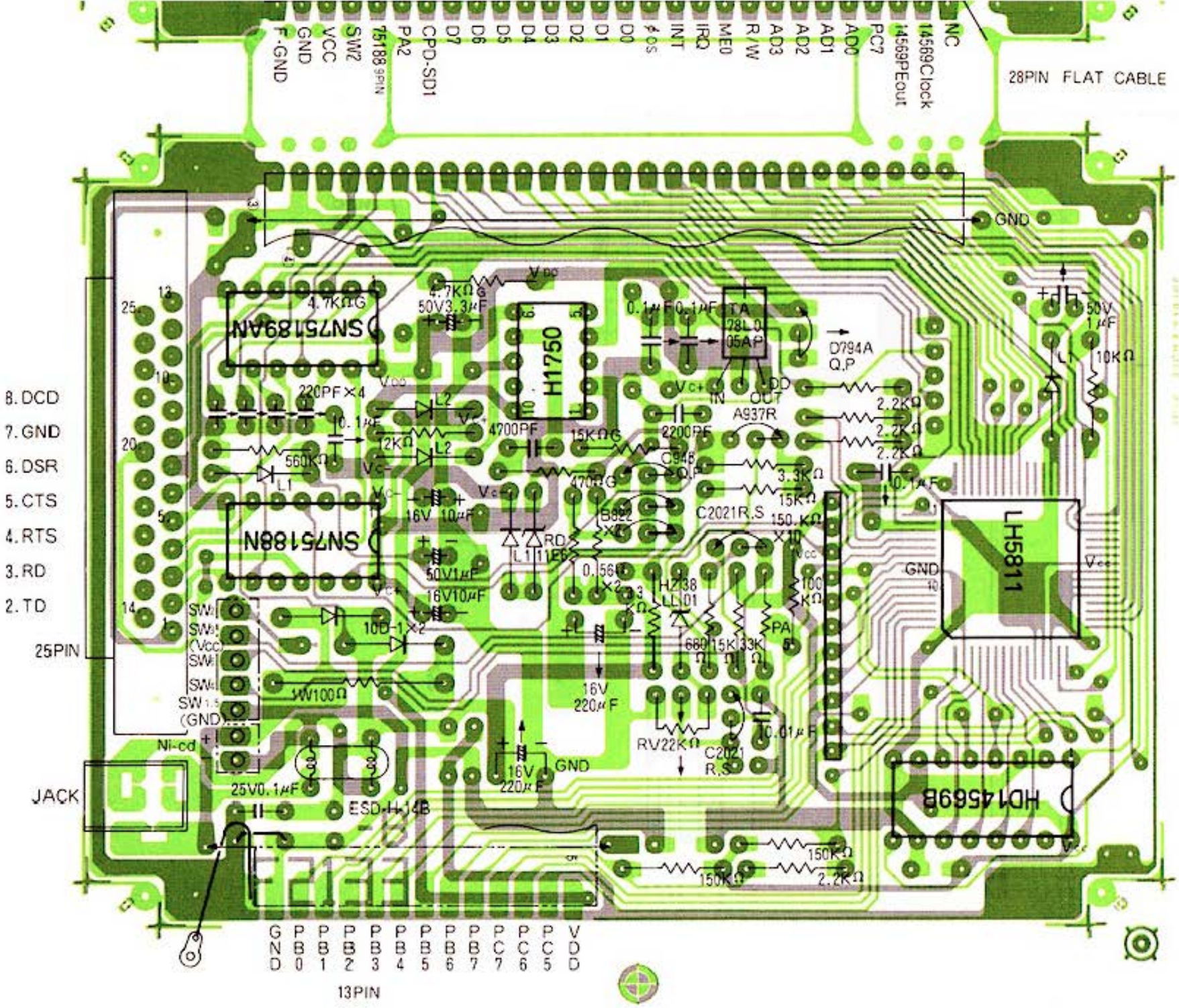


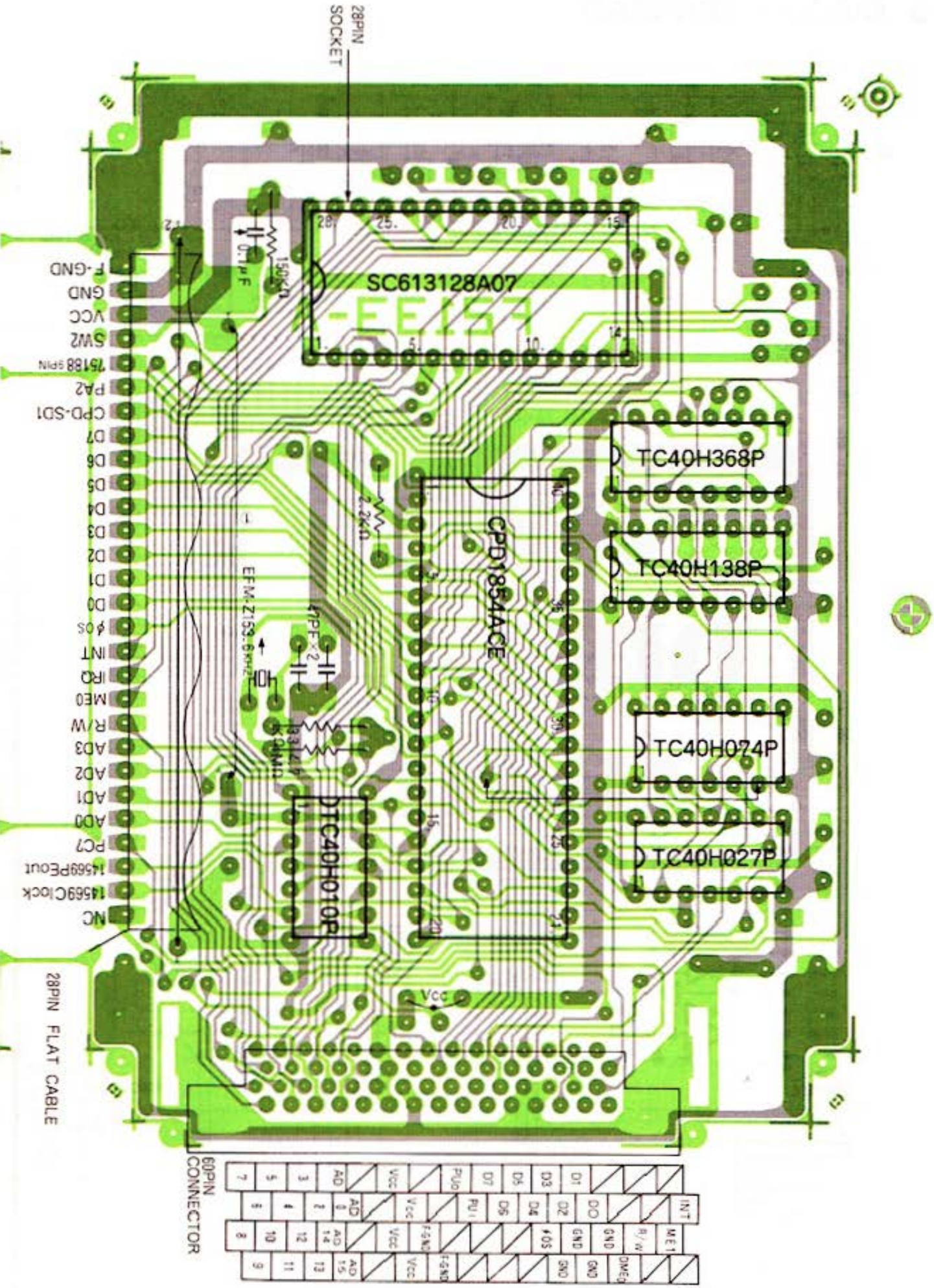
BLOCK DIAGRAM OF CDP1854A



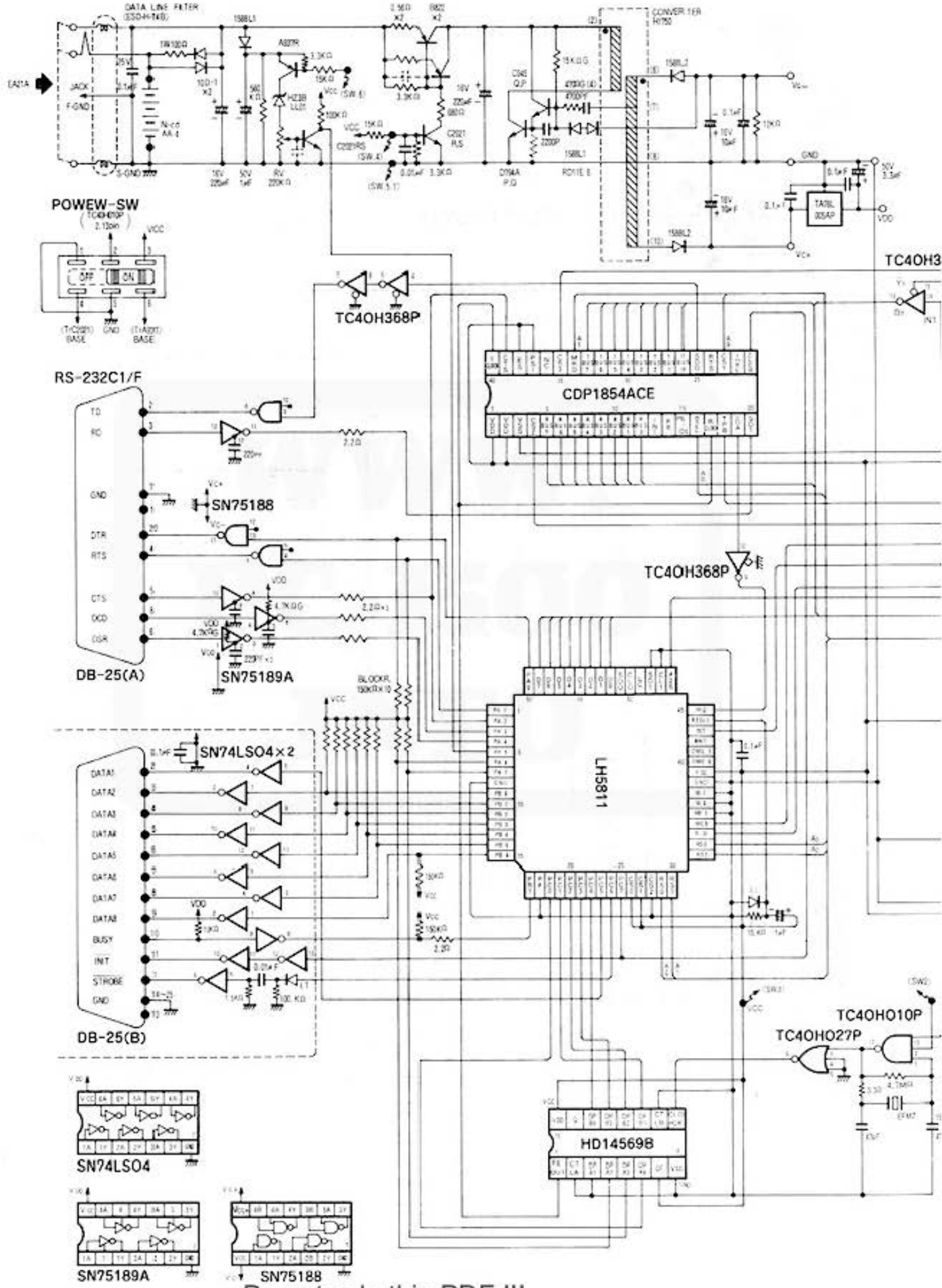


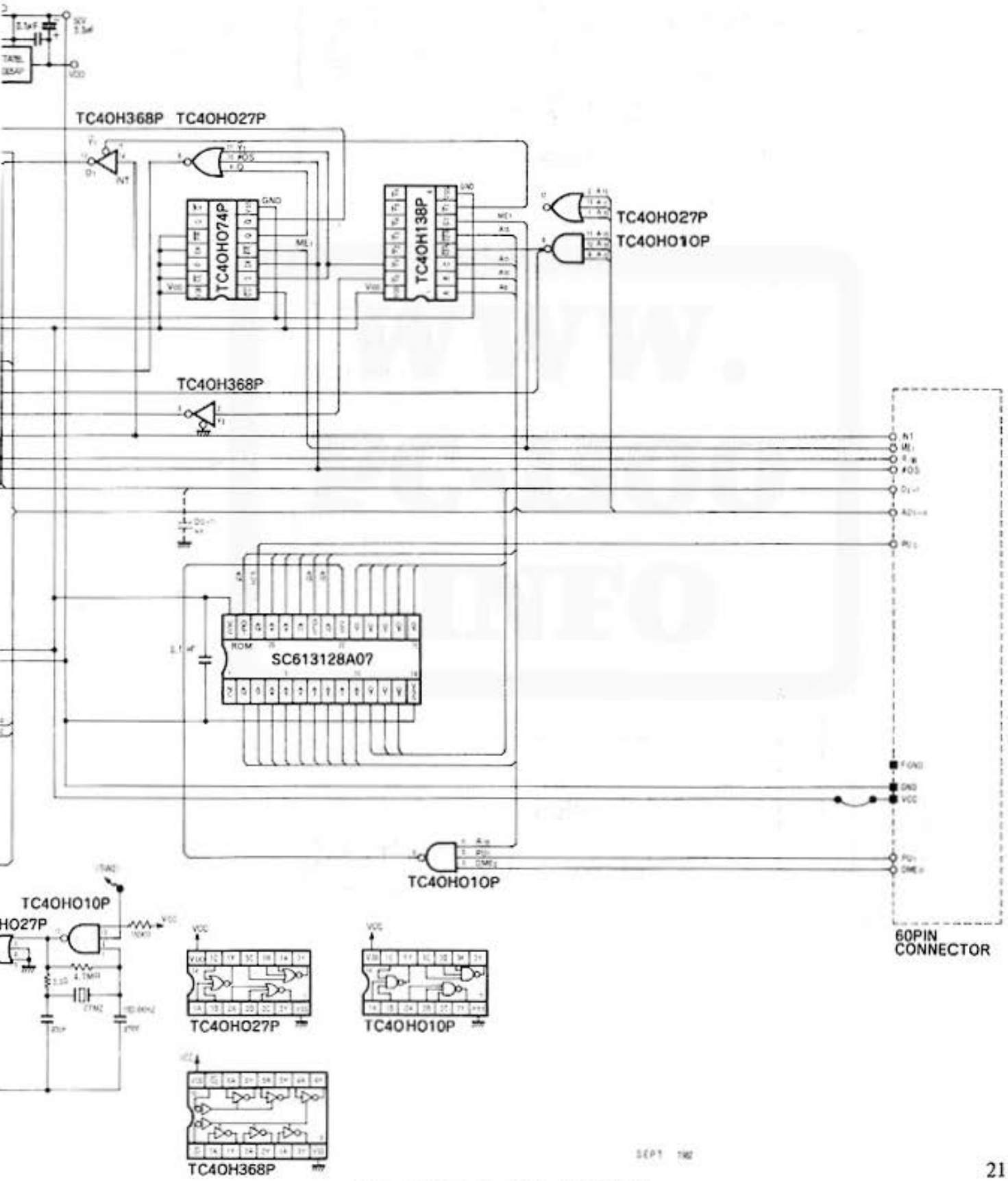
9. COLOR CHART



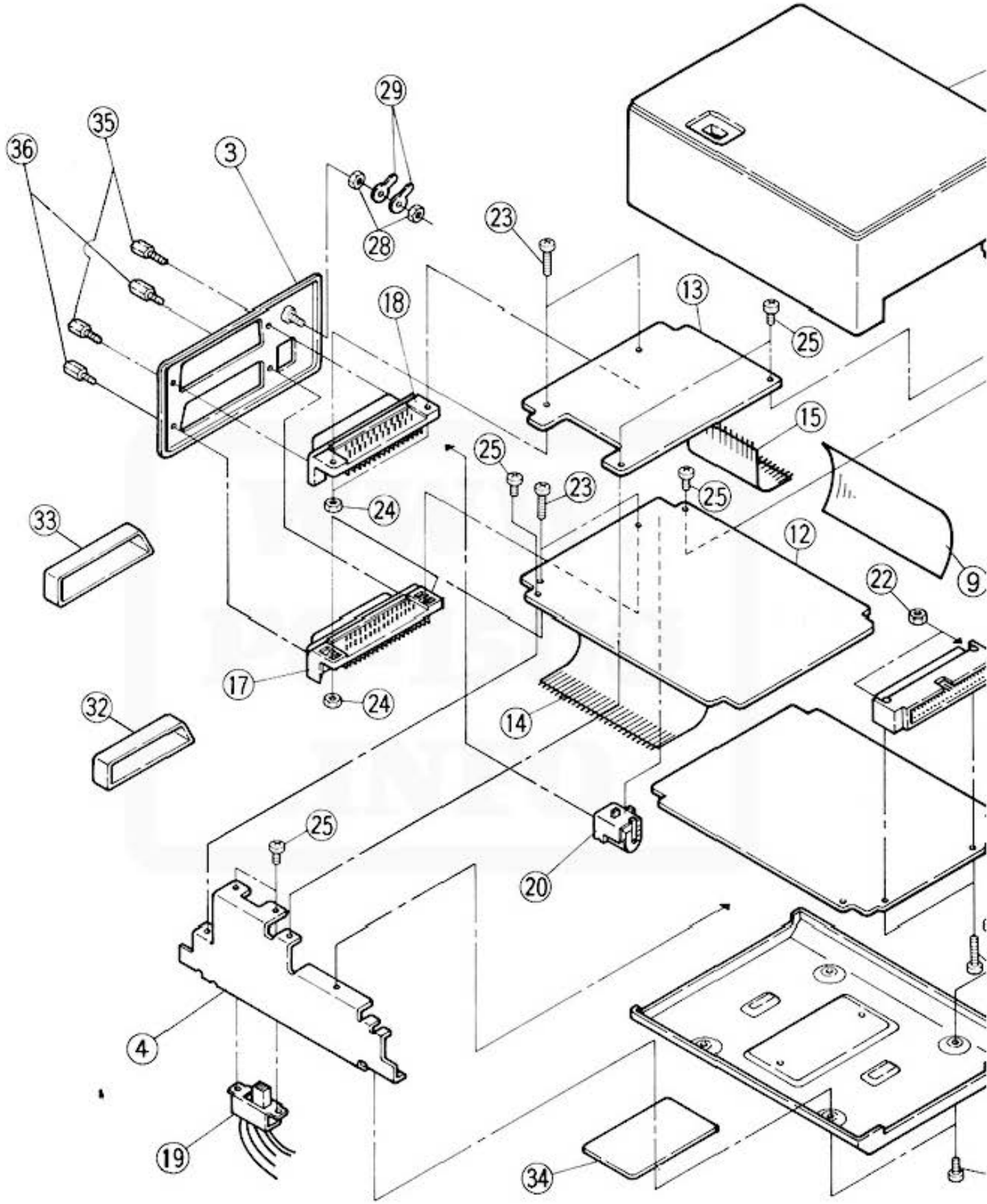


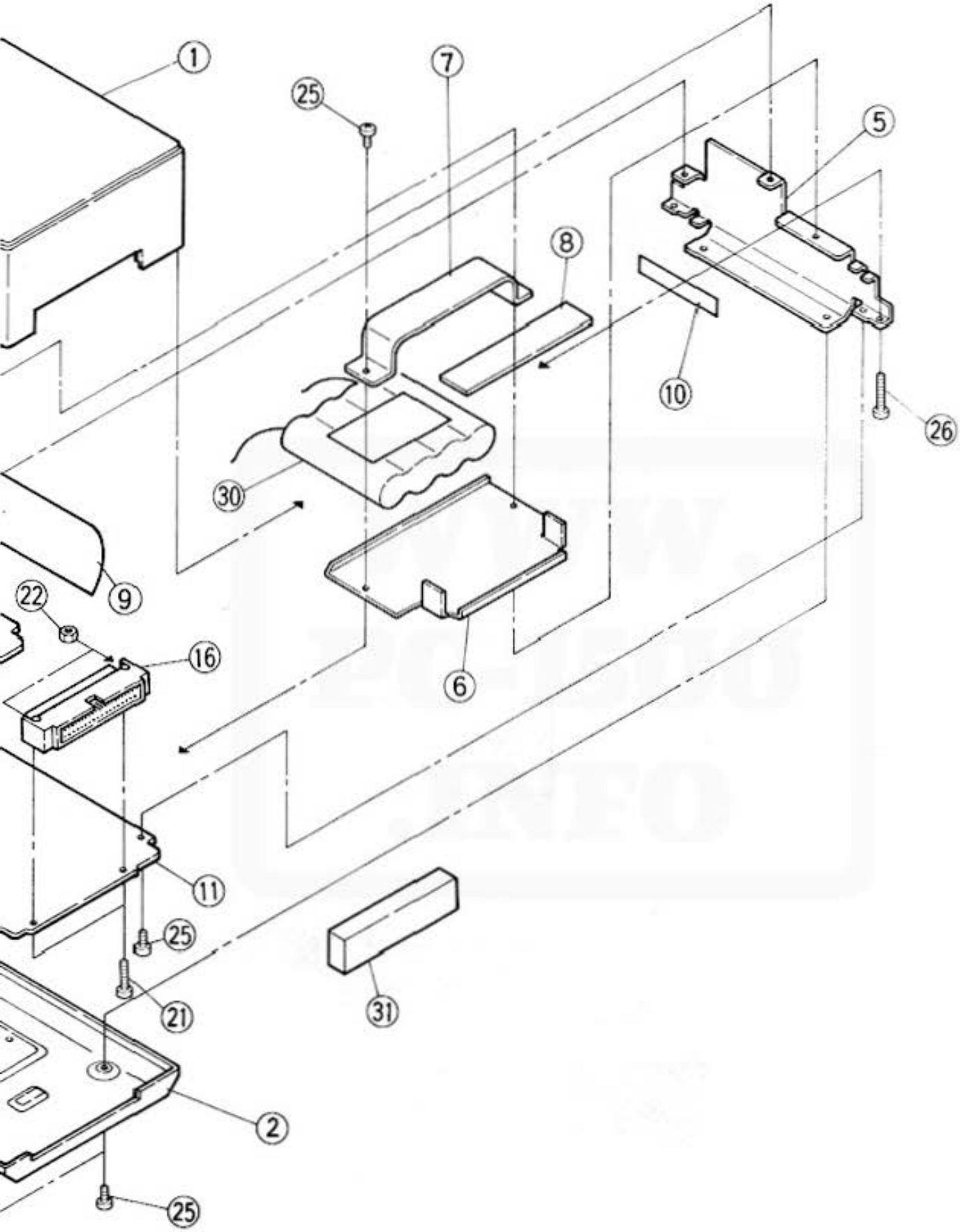
8. CIRCUIT DIAGRAM

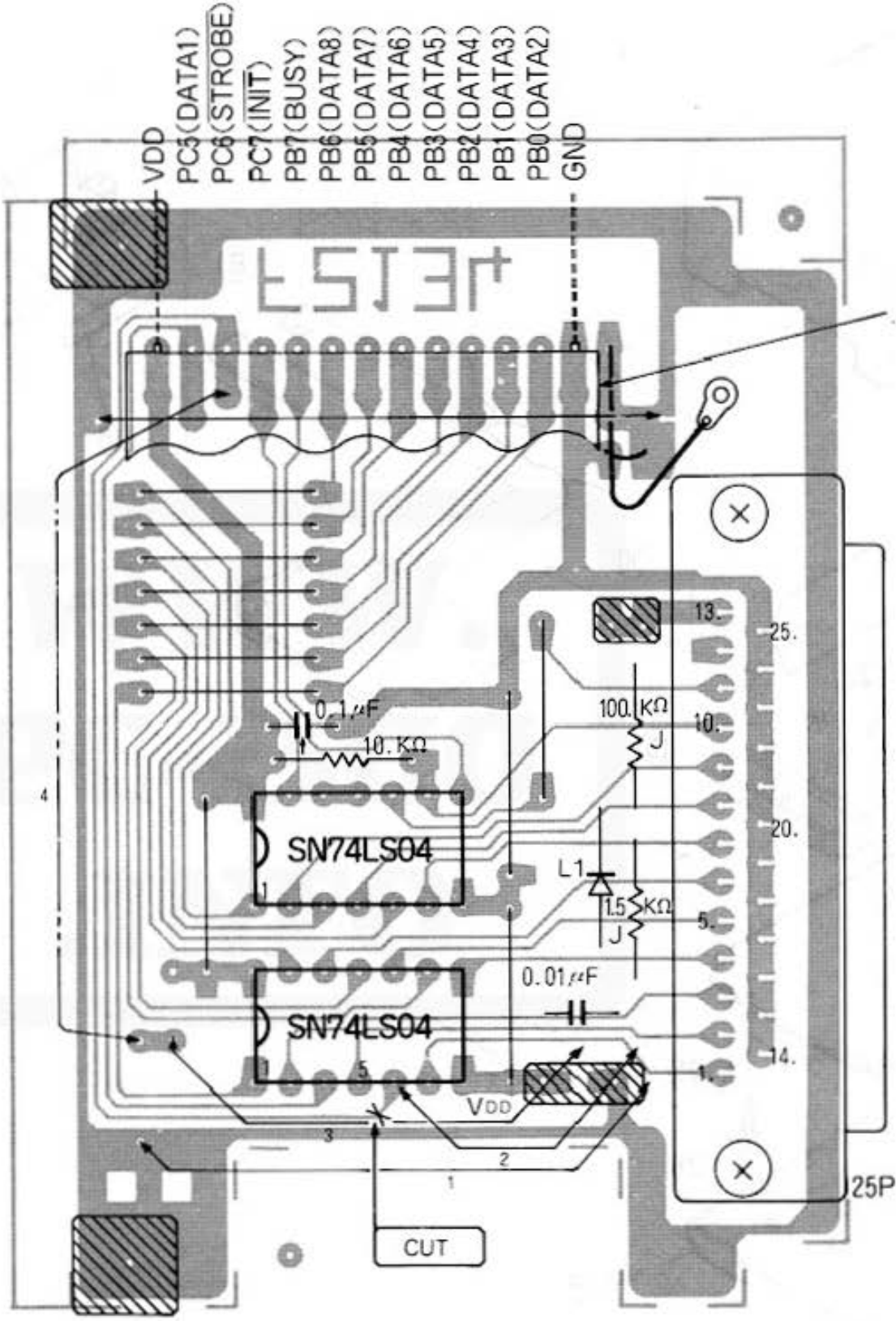


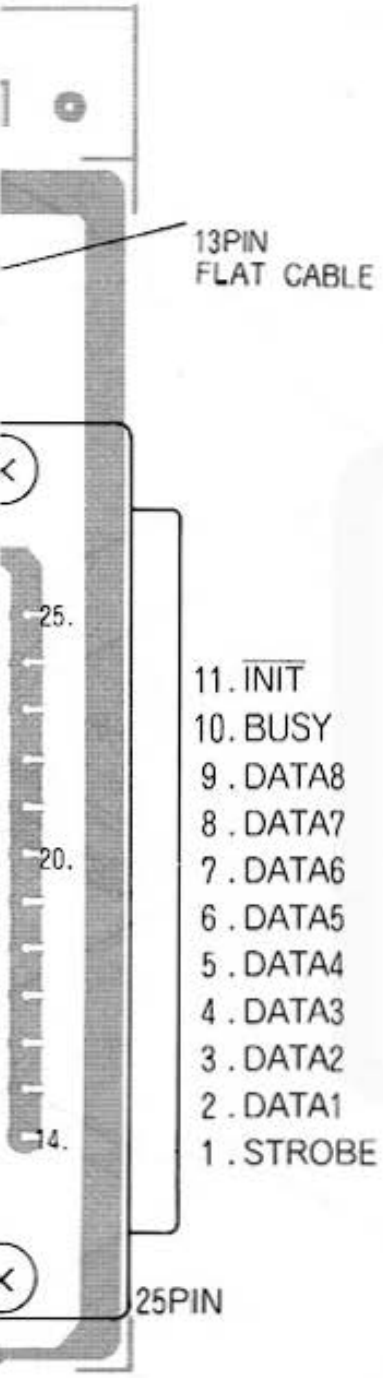


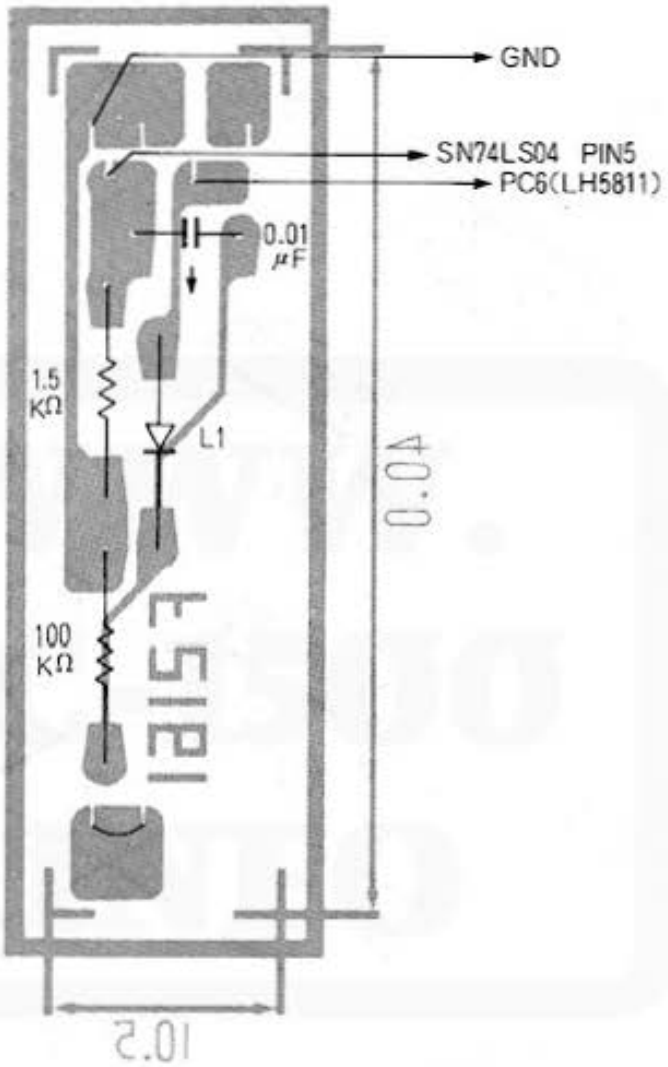
10. PARTS GUIDE











PARTS LIST

No.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
1	GCABB2681CCZZ	TOP CABINET	N	D	AM
2	GCABA2680CCZZ	BOTTOM CABINET	N	D	AL
3	HDECA2087CCZZ	DEC PANEL	N	D	AG
4	LANGT1476CCZZ	ANGLE-A	N	C	AE
5	LANGT1477CCZZ	ANGLE-B	N	C	AE
6	LANGT1475CCZZ	BOTTOM PANEL FOR Ni-cd BATTERY	N	C	AD
7	LFIX-1144CCZZ	HOLDER FOR FIXING OF Ni-cd BATTERY	N	C	AD
8	PCUSS1200CCZZ	CUSHION	N	C	AA
9	PZETL1469CCZZ	INSULATOR	N	C	AA
10	PZETL1470CCZZ	INSULATOR	N	C	AA
11	CPWBF2133CSNA	PWB UNIT (A) (RS232C)		E	
12	CPWBF2133CSNB	PWB UNIT (B) (RS232C)		E	
13	CPWBF2134CSNC	PWB UNIT (C) (PARAREL)		E	
14	QCNW-1233CCZZ	FLAT WIRE	N	B	AH
15	QCNW-1234CCZZ	FLAT WIRE	N	B	AD
16	QCNCM1295CC6J	60PIN CONNECTOR (M)		B	AV
17	QCNCW1305CC2F	25PIN CONNECTOR (RS232C)	N	B	BA
18	QCNCM1304CC2F	25PIN CONNECTOR (PARAREL)	N	B	BA
19	QSW-S1346CCZZ	POWER SWITCH	N	B	AG
20	QJAKC1003CCZZ	JACK FOR ADAPTOR		C	AD
21	XBBSF20P10000	SCREW (M2×10)		C	AA
22	XNESD20-16000	NUT			AA
23	XBBSD26P08000	SCREW (M2.6X8)		C	AA
24	XNESD26-20000	NUT		C	AA
25	XBPSD20P04000	SCREW (M2X4)		C	AA
26	XUPSD26P06000	SCREW (M2.6X6)		C	AA
28	XNESD30-24000	NUT		C	AA
29	QLUGE1008CCZZ	LUG		C	AA
30	CBATZ1054CC01	Ni-cd BATTERY		B	AZ
31	PCAPH1013CCZZ	CONNECTOR COVER	N	D	AD
32	PCAPH1015CCZZ	CONNECTOR COVER	N	D	AC
33	PCAPH1014CCZZ	CONNECTOR COVER	N	D	AD
35	LX-BZ1135CCZZ	SCREW (SPECIAL) OTHER CONTRY	N	C	AC
	LX-BZ1141CCZZ	SCREW (SPECIAL) USA, CANADA			
36	LX-BZ1135CCZZ	SCREW (SPECIAL)	N	C	AC
	CPWBF2133CSNA	PWB UNIT A			
	QCNCM1295CC6J	60PIN CONNECTOR (M)		B	AV
	QSOCZTD28ACZZ	IC SOCKET 28PIN		B	AH
	RCRSZ1045CCZZ	X'TAL 153.6KHZ	N	B	AH
	VCCCPU1HH470J	CAPACITOR (CERAMIC) 50V 47PF		C	AA
	VCTYPU1NX104M	CAPCITOR (SEMICONDUCTOR) 12V 0.1μF		C	AB
	VHICDP1854ACE	UART CDP1854ACE	N	B	BE

No.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
	VHiSC613128P7	ROM LSi	N	B	BG
	VHiTC40H010PN	iC TC40H010P	N	B	AF
	VHiTC40H027P1	iC TC40H027P		B	AF
	VHiTC40H074PN	iC TC40H074P		B	AL
	VHiTC40H138P1	iC TC40H138P		B	AN
	VHITC40H368PN	TC40H368P	N	B	AK
	VRD-ST2EY154J	RESiSTOR 150KΩ ¼W		C	AA
	VRD-ST2EY222J	RESiSTOR 2.2KΩ ¼W		C	AA
	VRD-ST2EY333J	RESiSTOR 33KΩ ¼W		C	AA
	VRD-ST2EY475J	RESiSTOR 4.7MΩ ¼W		C	AA
	XBPSD20P10000	SCREW (M2×10)		C	AA
	XNESD20-16000	NUT		C	AA
	CPWBF2133CSNB	PBW UNiT B			
	PZETL1172CCZZ	iNSULATOR		C	AA
	QCNCM1254CC0B	CONNECTOR 2PiN (M)		B	AC
	QCNOM2331RC0E	CONNECTOR 5PiN (M)		B	AF
	QCNCW1305CC2F	CONNECTOR 25PiN (F)	N	B	BA
	QCNCW-1233CCZZ	WiRE	N	B	AH
	QJAKC1003CCZZ	JACK FOR ADAPTOR		C	AD
	RC-EZ105ACC1H	CAPACiTOR 50V 1μF		C	AB
	RC-EZ106ACC1C	CAPACiTOR 16V 10μF		C	AB
	RC-EZ227BCC1C	CAPACiTOR 16V 220μF		C	AC
	RC-EZ335ACC1H	CAPACiTOR 50V 3.3μF		C	AB
	RFiLN1005CCZZ	FiLTER	N	C	AH
	RMPTC0154QCKJ	RESiSTOR 150KΩ×10 1/16W		B	AD
	RTRNH1750CCZZ	CONVERTER TRANSFORMER	N	B	AK
	RVR-MB410QCZZ	VARiABLE RESiSTOR 22KΩ		B	AD
	VCKYPU1HB103K	CAPACiTOR (CERAMiC) 50V 0.01μF		C	AA
	VCKYPU1HB221K	CAPACiTOR (CERAMiC) 50V 220PF		C	AB
	VCKYPU1HB222K	CAPACiTOR (CERAMiC) 50V 2200PF		C	AA
	VCKYPU1HB472K	CAPACiTOR (CERAMiC) 50V 4700PF		C	AA
	VCTYPU1EX104M	CAPACiTOR (SEMiCONDUCTOR) 50V 0.1μF		C	AB
	VCTYPU1NX104M	CAPACiTOR (SEMiCONDUCTOR) 12V 0.1μF		C	AB
	VHDDS1588L1-1	DiODE		B	AD
	VHDDS1588L2-1	DiODE		B	AB
	VHD10D1////-1	DiODE		B	AD
	VHEHZ3BLL01-1	ZENER DiODE		B	AD
	VHERD11E6//-1	ZENER DiODE		B	AC
	VHiHD14569B-1	iC HD14569B	N	B	AN
	VHiLH5811//-1	iC LH5811		B	AZ
	VHiSN75188N-1	iC SN75188N		B	AM

No.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
	VHiSN75189A-1	IC SN75189A		B	AP
	VHiTA78L005AP	IC TA78L005AP		B	AH
	VRD-ST2EYR56J	RESISTOR 0.56Ω ¼W 5%		C	AA
	VRD-ST2EY103J	RESISTOR 10KΩ ¼W 5%		C	AA
	VRD-ST2EY104J	RESISTOR 100KΩ ¼W 5%		C	AA
	VRD-ST2EY123J	RESISTOR 12KΩ ¼W 5%		C	AA
	VRD-ST2EY153G	RESISTOR 15KΩ ¼W 5%		C	AA
	VRD-ST2EY153J	RESISTOR 15KΩ ¼W 5%		C	AA
	VRD-ST2EY154J	RESISTOR 150KΩ ¼W 5%		C	AA
	VRD-ST2EY222J	RESISTOR 2.2KΩ ¼W 5%		C	AA
	VRD-ST2EY332J	RESISTOR 3.3KΩ ¼W 5%		C	AA
	VRD-ST2EY333J	RESISTOR 33KΩ ¼W 5%		C	AA
	VRD-ST2EY471G	RESISTOR 470Ω ¼W 2%		C	AA
	VRD-ST2EY472G	RESISTOR 4.7KΩ ¼W 2%		C	AA
	VRD-ST2EY564J	RESISTOR 560KΩ ¼W 5%		C	AA
	VRD-ST2EY681J	RESISTOR 680Ω ¼W 5%		C	AA
	VRS-PT3AB101J	RESISTOR 100 Ω 1W 5%		C	AB
	VS2SA937-R/-1	TRANSISTOR (2SA937)		B	AC
	VS2SB822-//-1	TRANSISTOR (2SB822)		B	AD
	VS2SC2021-RSC	TRANSISTOR (2SC2021)		B	AF
	VS2SC945-P/QC	TRANSISTOR (2SC945)		B	AC
	VS2SD794AP/QC	TRANSISTOR (2SD794)	N	B	AE
	XBBSD26P08000	SCREW (M2×8)		C	AA
	XNESD26-20000	NUT		C	AA
	CPWBF2134CSNC	PWB UNIT C			
	QCNCM1304CC2F	CONNECTOR 25PIN (M)	N	B	BA
	QCNW-1234CCZZ	FLAT CABLE	N	B	AD
	VCTYPU1NX104M	CAPACITOR (SEMICONDUCTON) 12V0.1μF		C	AB
	VHiSN74LS04-1	SN 74LS04 IC		B	AE
	VRD-ST2EY103J	RESISTOR 10KΩ ¼W		C	AA
	XBBSD26P08000	SCREW (M2×8)		C	AA
	XNESD26-20000	NUT		C	AA
	TCAUH1201CCZZ	CAUTION LABEL	N	D	AA
	TLABB1713CCZZ	NAME LABEL	N	D	AB
	TLABN1152CCZZ	SER NO LABEL		D	AA
	LHLDZ1181CCZZ	HOLDER A	N	C	AN
	LHLDZ1182CCZZ	HOLDER B	N	C	AL
	LPLTP1102CCZZ	TEMPLATE	N	D	AL
	PGUMS1450CCZZ	CUSHION FOR IC	N	C	AA
	QCNCW1311CC01	CONNECTOR 2PIN (F)	N	B	AF

No.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
	QCNCW1312CC01	CONNECTOR 5PIN (F)	N	B	AD
	DUNT-3710CC02	EA-21A USA CANADA SD			AW
	DUNT-3711CC02	EA-21A MA			AX
	DUNT-3712CC02	EA-21A MB			AY
	DUNT-3713CC01	EA-21A MV			AY
	DUNT-3714CC02	EA-21A SB			AY
	DUNT-3715CC01	EA-21A SC			BA
	CUNT-3716CC01	EA-21A SE			BC
	DUNT-3717CC01	EA-21A SH			BA
	DUNT-3718CC01	EA-21A SK			AY
	CUNT-3719CC01	EA-21A SM			BC
	DUNT-3721CC01	EA-21A SN			AZ
	TINSE3719CCZZ	INSTRUCTION MANUAL USA	N	D	BF
	TINSM3720CCZZ	INSTRUCTION MANUAL OTHERS	N	D	BR
	SPAKA7406CCZZ	PACKING AD FOR CE158	N	D	EF
	SPAKA7407CCZZ	PACKING AD A FOR ATACHMENT	N	D	DC
	SPAKA7408CCZZ	PACKING AD B FOR ATACHMENT	N	D	DB
	SPAKC7610CCZZ	PACKING CASE	N	D	AH
	SPAKC7411CCZZ	PACKING CASE (USA ONLY)	N	D	AH

SHARP CORPORATION
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Reliability & Quality Control Department
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